SONY®

DXC-1800P

TRAINING TEXT

CONTENTS

I. INTRODUCTION

1-1. Line-up

The DXC-1800P is the successor to the DXC-1640P in the line-up of Trinicon cameras. It incorporates significant improvements which can be summarized as follows :

1. Picture quality
2. Operational convenience
3. Combined portable and studio facilities in a small package.

The better picture quality is due primarily to the saticon photoconductive layer used in the SMF 2/3 inch tube : no lag, low retention and more sensitive. The ABO circuit ensures good highlight handling. The signal-to-noise ratio was increased by 3dB through the use of a new FET in the pre-amp.
Beside horizontal, there is also a one-line vertical aperture correction.
Power-consumption is the same as for previous models and size and weight are slightly less. Several new features make operation easy.

- auto white balance (microprocessor)
- fader
- ABL
- three calibrated gain steps (0,6,12dB)
- motor-zoom (slow-fast)
- complete alarm system
    - VTR indicator
    - low light
    - VO or DXC low battery
    - colour-bar generator
    - stable shoulder brace
    - left and right viewfinder mounting
    - quick start.

For studio operation, the DXC-1800P can be connected to the control unit CCU-1800P through a standard CCQ cable, which is less expensive and easier to handle than CCY, CCX, CCW.
Nevertheless, it carries power, gen-lock signal, return video, actual camera signal, tally/intercom, and remote control of 7 analog and 7 switching functions.
This is made possible by the two new systems : one is the gen-locked sync generator and the combination of gen-lock and return video on one coax cable, the other is the digital data-link and the two microprocessors in the camera and the control unit.

It is also possible to use the DXC-1800P in a mixing set-up without the CCU : a gen-lock input and SC/H phase controls are provided on the camera itself.

The DXF40CE studio viewfinder has a 4 inch screen, tally/intercom and can be tilted and rotated in all directions.

1-2. Overview of circuitry

The DXC-1800P is housed in a sturdy, cast-alu cabinet with an integrated pre-amplifier case. The circuits are functionally placed on few boards that are easily accessible.

To achieve compact circuitry, a whole new series of custom IC's was designed as shown in the table below. The BX are vertically-mounted in-line IC's. Beside these SONY IC's, standard low-power op-amps and digital IC's are used.

Comparator : NJM2903, µPC311C,
op-amps µPC339, µPC4557/8, TL064/072/048
(JFET input), CMOS, analog switches
TC4051/53, TL607CP.

Double-sided PCB's, mini, metal-film potentiometers and 1/16W vertically mounted resistors also contribute to save space.

POWER	PW53	switching ref. 9.5V + series reg 6.5V		
SG	SG 34	CX7903 SC COMP,...		
		CX773A SG		(1)
DEFL	DF10	BX369		(1)
PA	PA12	2SK152		(1) (2)
PROCESS	PR25	gain CTL, γ ,CLP	CX810	(1)
		AP. CORR:H	CX815	(1)
		V	BX311	new
			µA796	"
			SN16913P	"
CHROMA	CR11	amp (DL drive)	CX816	(1)
		index mod/alt	CX811	(1)
		demod/WB		
		H/V SAWT	BX378	(1)
		Ind amp	BX306	new
		mod/burst gen.	CX873	new
		CB BLK, PED	CX814/1	
OUTPUT	CR11	fader/out	CX814-/2	(1)
VTRinterface	CR11		CX518	(2)
CCU	CR11	microprocessor	HD44750A14	new
VF	VF12,13	BX311		
		CX104		
		µPC575		

(1) also in HVC2000P
(2) " " DXC-1640P
IC specifications are found in the appendix.

2. POWER

2-1. Power consumption

The DXC-1800P is powered from a 12V unregulated supply which may vary between 15 and 10.8 Volts. Current consumption changes with supply voltage as shown in following table.

SUPPLY VOLTAGE	CURRENT CONS.	POWER
15V	1.08A	16.2
14V	1.12A	15.7
13V	1.17A	15.2
12V	1.22A	14.6
11.5V	1.28A	14.7

An important parameter for portable sets is the operating time on one (fully charged) battery. This is illustrated in the figures and tables below for the DXC-1800P camera and associated system components.

The values are for optimum conditions, room temperature, high charging voltage, low "battery-cut", regular cycling. A 20 to 40% lower capacity is to be expected under outdoor conditions, infrequent charging and offset charge-discharge limits.

The operating times are given only for the most important combinations.

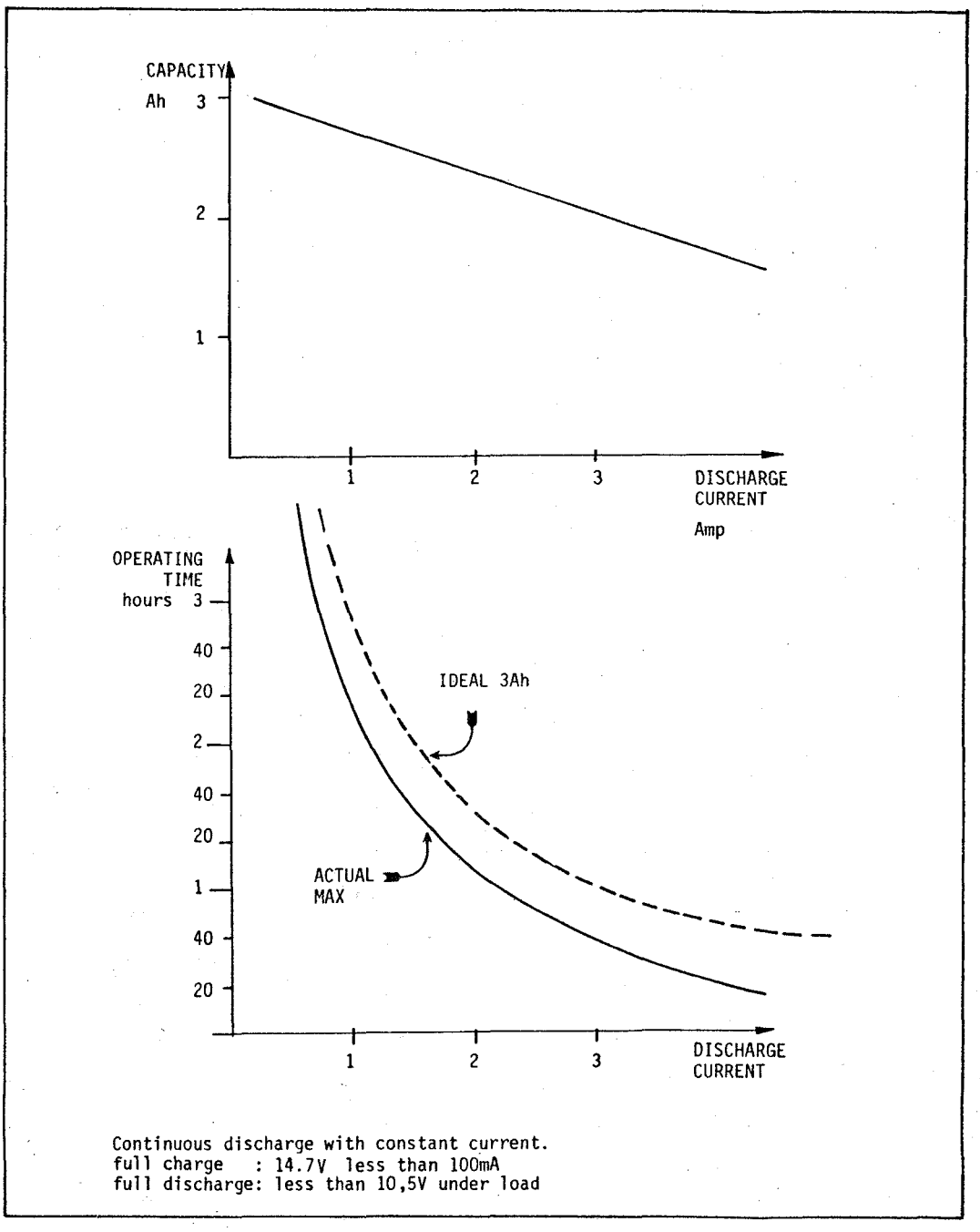


Fig. 2-1. BP20A/BP60A Capacity

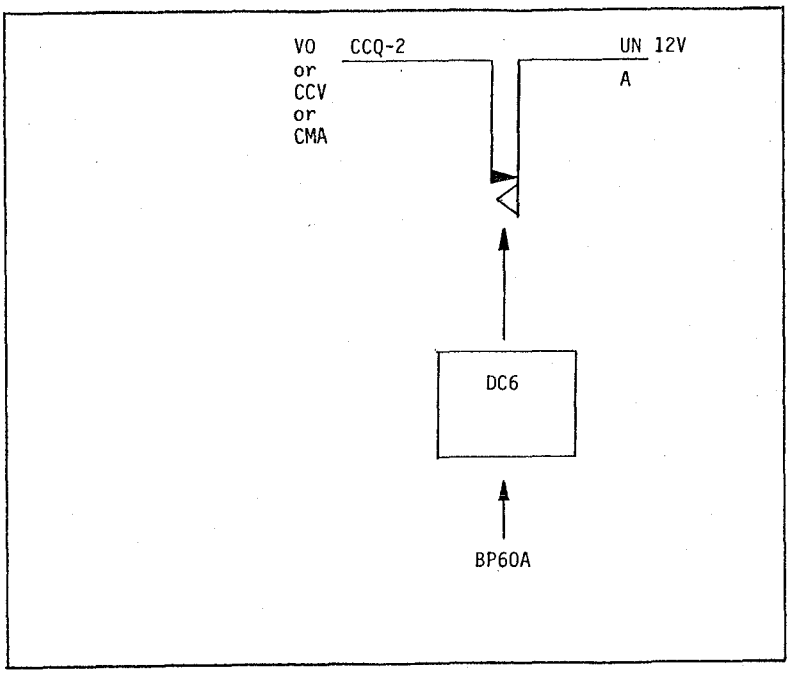
CONSUMPTION OF SONY PORTABLE VTR's AND CAMERAS

	POWER CONS W	CURRENT CONS A
AVC 3420CE	8W	0.67A
AVC 3450	7W	0.58A
DXC 1600P	21W	1.75A
DXC 1610	12W	1A
DXC 1640	12W	1A
DXC 1800	11W	0.9A *
HVC 2000P	8.3W	0.7 *
AV 3420CE		
VO 3800P	27.6W	2.3A
VO 4800P	11W	0.9A *
DXF40CE	11W	0.9A
CCU1800P	3.7W	0.31A

* These sets have a switching regulator, and current consumption increases as the supply voltage goes down.

	CURRENT CONS	OPERATING TIME	
		MAX	ACTUAL
DXC 1800P	1.25A	2h25	1h50
VO 4800P (RECORD mode)	0.9A	3h20	3h
VO 4800P + DXC 1800P	2.15A	1h25	1h
DXC 1800P + DXF40CE	2.15A	1h25	1h
CCU 1800P + DXC40CE	1.2A	2h30	2h
CCU 1800P + DXC 1800P + 2 x DXFCE	3.35A	0h55	0h35

2-2. DC6



Power may come through pin 2 of the CCQ cable or through the DC-in connector. The DC6 battery adaptor has following functions (DC8 circuit board):

- power switch
- battery meter
- low-battery detect and alarm generator
- under-cut

Fig. 2-2.

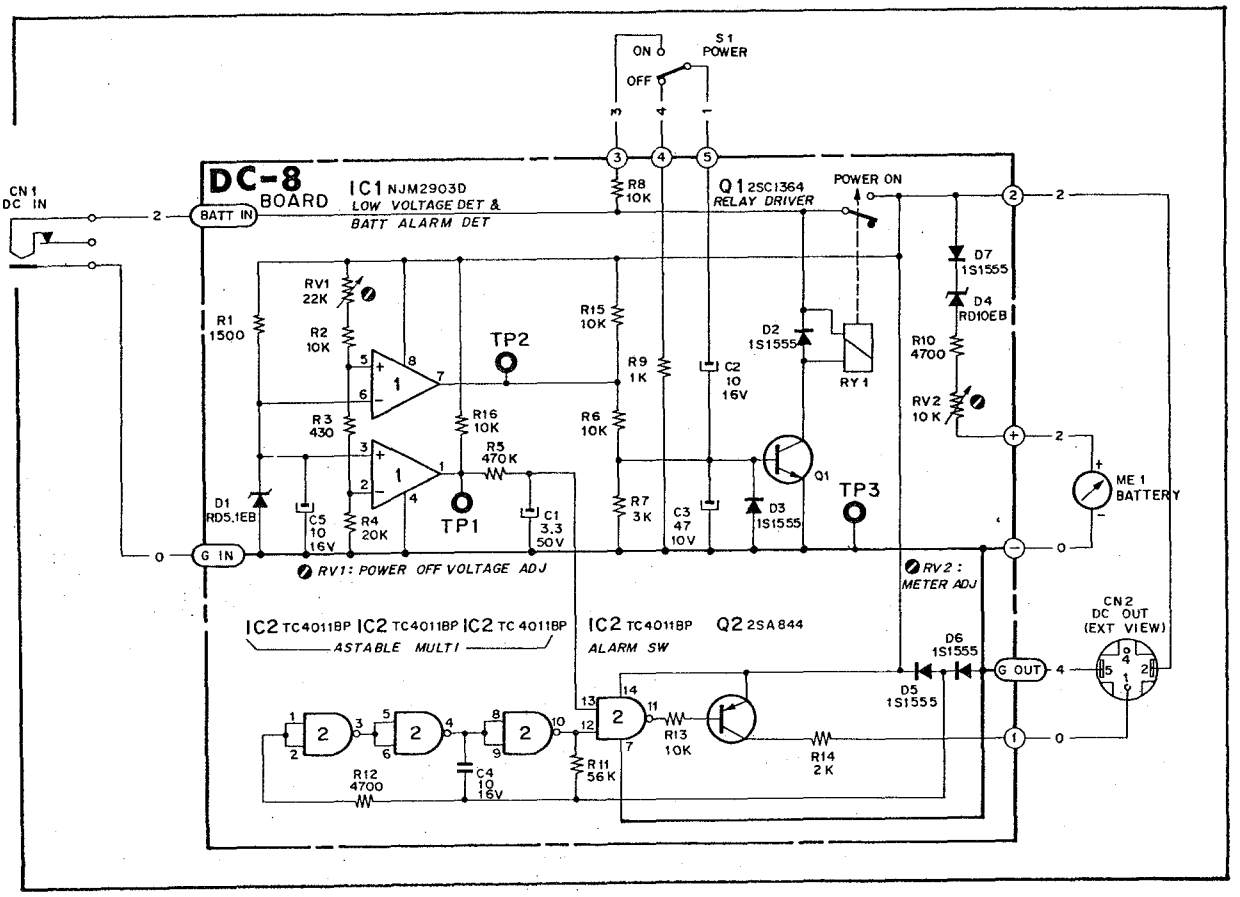
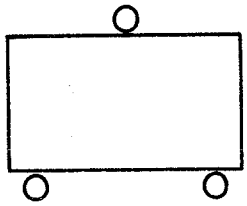


Fig. 2-3. DC-6 Schematic diagram

At power-on, Q1 is switched on (base-current through C2) and RY1 activates. Q1 remains on through R15 and R6. When the battery voltage drops below 11.0V, IC1-pin 1 goes high and the 1Hz square wave at IC2-pin 10 is passed. Via buffer Q2 and the new type of DC-in connector the alarm signal goes to the battery lamp in the viewfinder.



BATTERY

If the battery voltage drops below 10.8V, IC1-pin 7 (TP2) goes low and power is cut off. Both thresholds are set with the same adjustment.

2-3. Regulator system

The DXC 1800P operates basically from +9 and -5V for the analog circuits, and +5 for the digital ones. These voltages are derived in several steps.

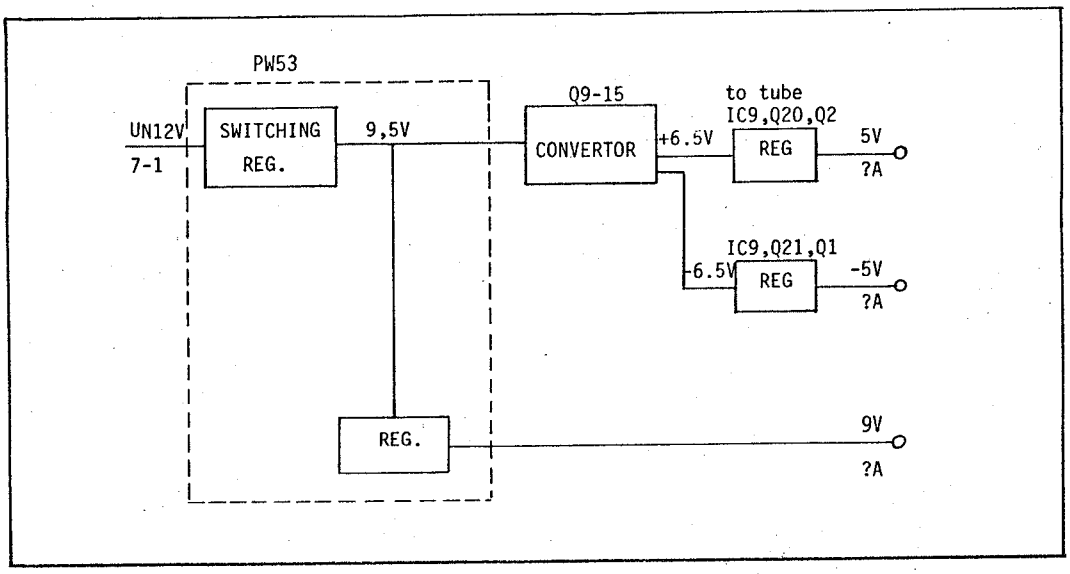


Fig. 2-4.

The main (switching) regulator produces 9.5V regulated and has a very good efficiency. Another series-type regulator produces 9V with low ripple for the video circuits. Both blocks are located on the PW53 board (shielded).

The switching convertor on the DF10 board is powered from the 9.5V and produces all voltages necessary to operate the tube, plus +6.5 and -6.5V which are then regulated to give +5 and -5V.

The switching regulator is new in the DXC line of cameras, so let us review the basic principles.

Fig. 2-5. shows the basic forward switching converter.

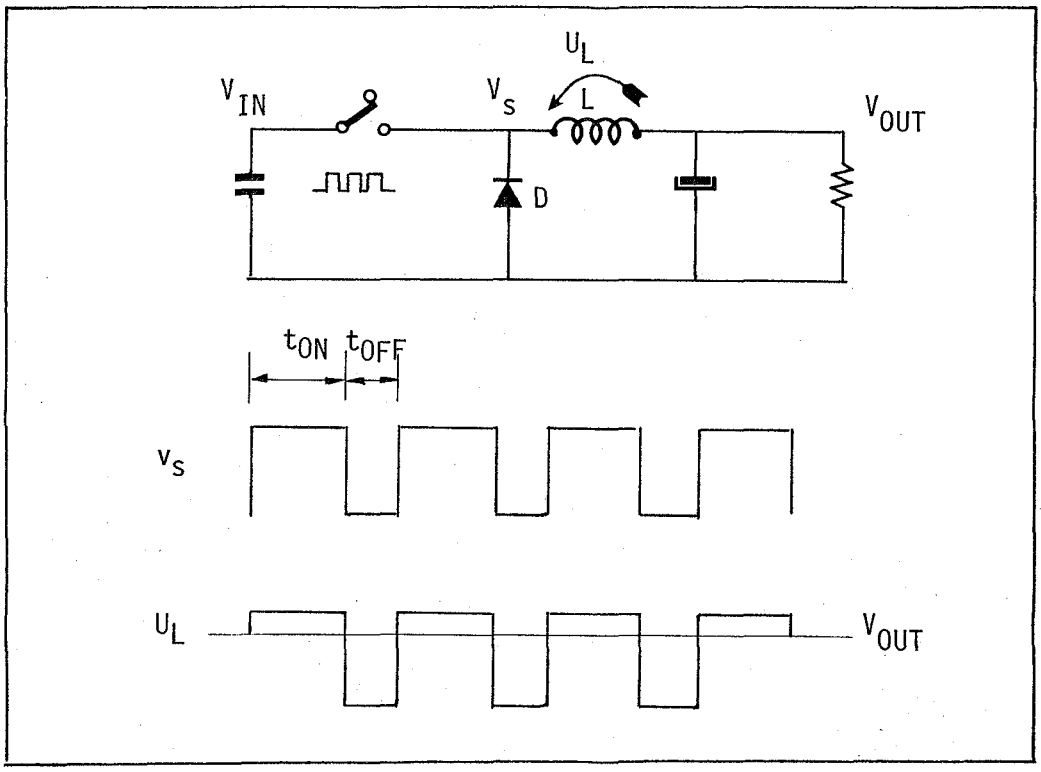


Fig. 2-5.

The inductance L must be high enough so that the current changes are small.

In equilibrium, the average voltage across the coil must be zero. (Otherwise the current will increase continuously.)

$$V_L dt = 0$$

$$(V_{IN} - V_{OUT})\ t_{ON} - V_{OUT}\ t_{OFF} = 0$$

$$V_{OUT} = \alpha V_{IN}$$

$$\alpha = \text{duty cycle}$$

And, since there are no losses (approx.)

$$P_{OUT} = P_{IN}$$

$$I_{\underset{AV}{IN}}\ V_{IN} = I_{OUT}\ V_{OUT}$$

$$I_{\underset{AV}{IN}} = \alpha I_{OUT}$$

A more useful way to write this relationship is :

$$I_{\underset{AV}{IN}} = \frac{I_{OUT}\ V_{OUT}}{V_{IN}}$$

Since output current and voltage are constant, the current consumption is inversely proportional to the input voltage !

Regulation is obtained by varying the duty cycle.

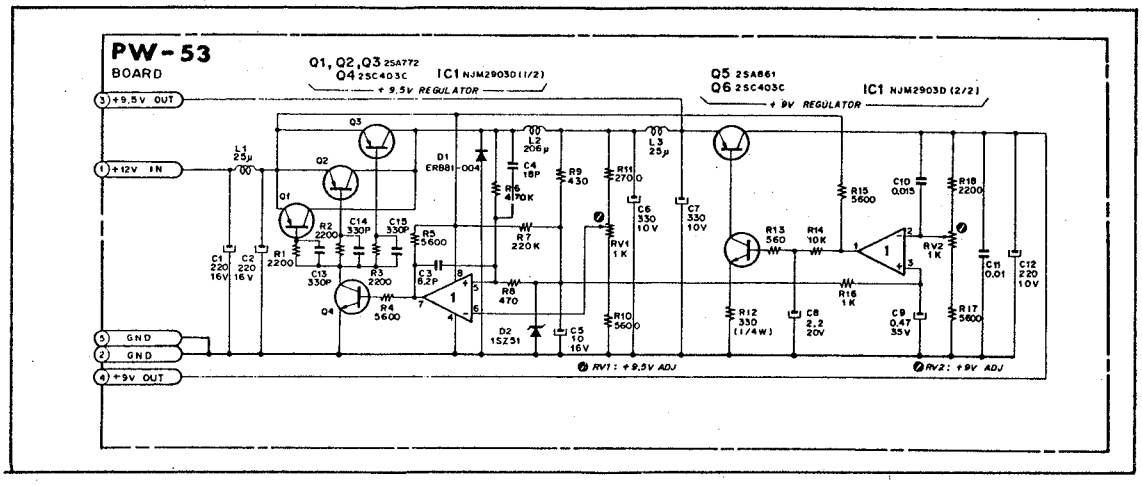


Fig. 2-6. PW-53 board +9.5V +9V Regulator. Schematic Diagram

Fig. 2-6. shows the actual circuit.

Three low-power, high frequency transistors 2SA772 are used in parallel as a switch. The diode is also a fast type so as to reduce power dissipation during switching. The square wave is generated and modulated in one circuit using an NJM2903 comparator.

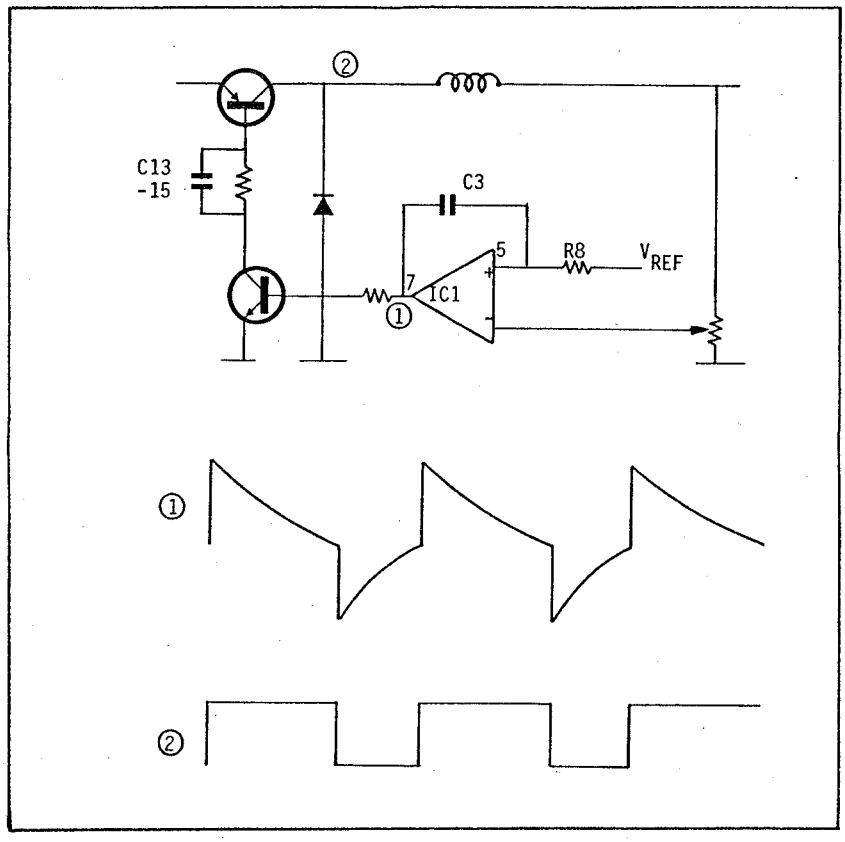


Fig. 2-7.

The time - constant R_8 C_3 determines the switching frequency.

The 9V switching regulator in the DXF3CE is of the same type but uses only one 2SA773 transistor.

3. SYNC GENERATOR

3-1. General

The DXC-1800P sync generator is a completely new design using two SONY custom IC's.

CX773A sync generator
CX7903 gen-lock adapter

They are implemented in C-MOS technology, and operate on a 5V supply. Use is universal : logical inputs switch between NTSC, PAL, PALM and SECAM modes, int/ext and different modes of ext. sync.

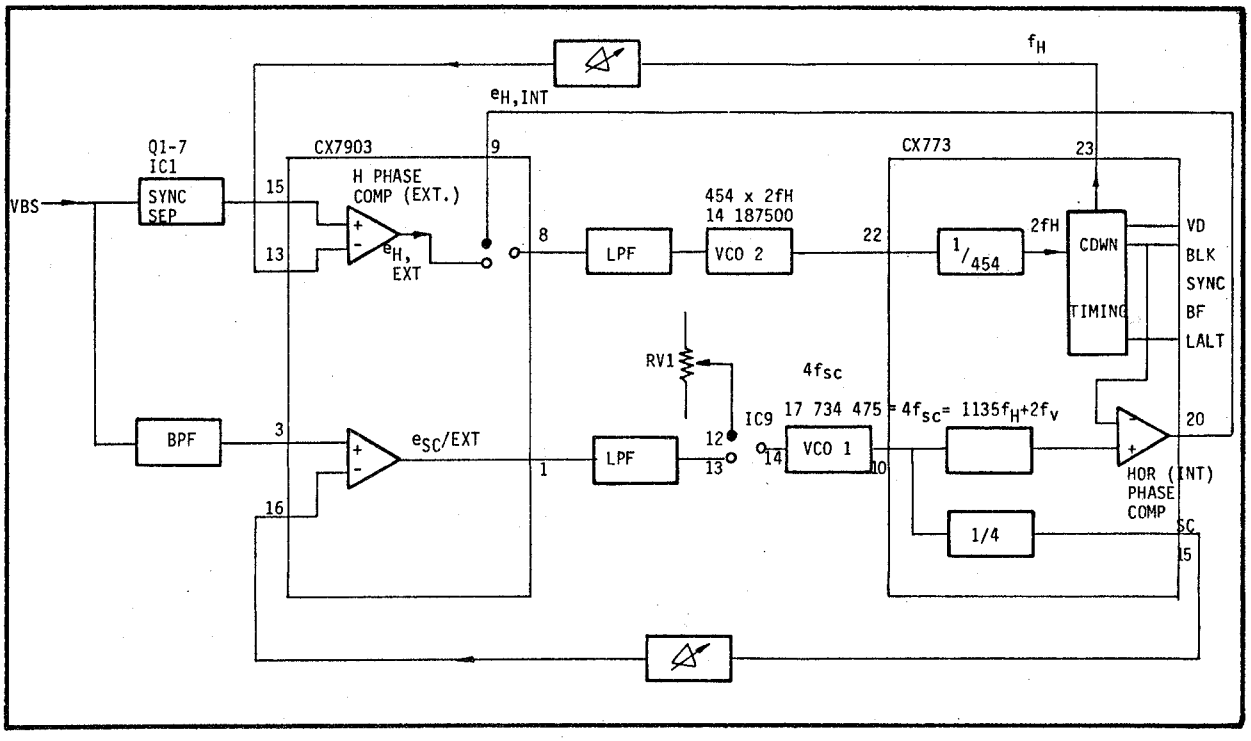


Fig. 3-1. Sync generator simplified block diagram.

The SG34 uses two supply voltages :

9V, consumption 30mA
and 5V, consumption 86mA.

3-2. Internal

In internal sync mode, only the CX773A is involved. Because of the quarter line offset of the PAL subcarrier and compatibility requirements, the design uses two clock oscillators. VCO1 free-runs at four times subcarrier frequency. Bias is adjusted with RV1. Stability of this oscillator is critical since all sync pulses are related to it. ($f_{SC} \pm 10Hz$). The VCO2 frequency is 454 times $2f_H$ ($\cong$ 455 x $2f_H$ for NTSC mode Xtal) and is used to derive VD, HD, BLK, SYNC and BF. VCO2 is controlled by a phase-locked-loop in such a way that HD and VD are properly related to SC.

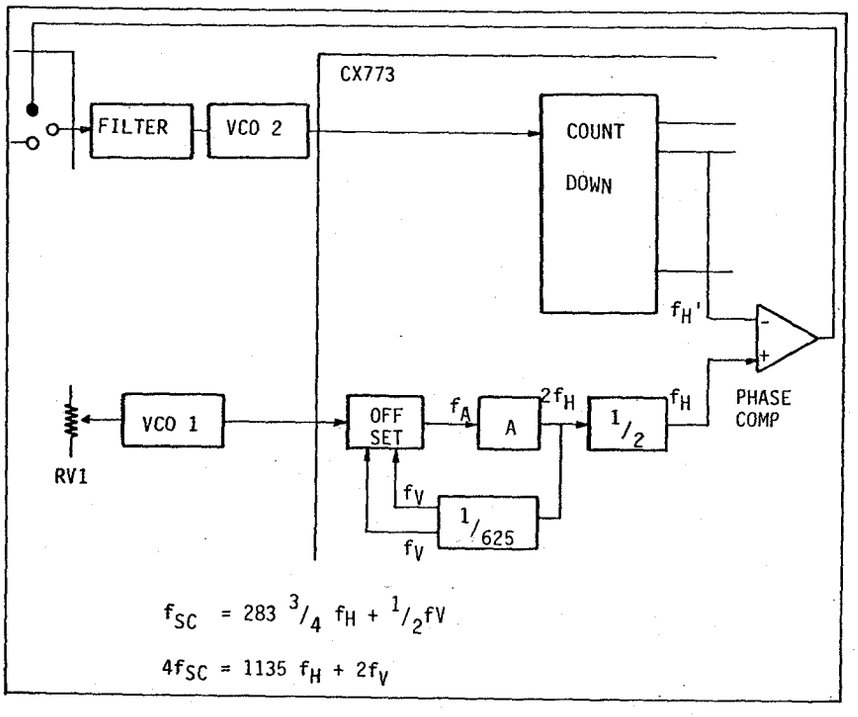


Fig. 3-2. Sync generator in internal mode.

If the loop is locked then the frequencies at the input of the phase comparator must be exactly equal. The countdown in block A is such that

$$f_H = \frac{f_A}{1135}$$

In the block "OFFSET" each incoming f_V pulse removes one pulse from the $4f_{SC}$ pulse train.

$$4f_{SC} = f_A + 2f_V = 1135f_H + 2f_V.$$

The horizontal phase comparator used is inside CX773A but the phase error passes through an analog switch inside CX7903.

3-3. External

In external mode the same two VCO's are used but now they are locked independently to B/W and colour sync of the incoming "VBS" video signal.

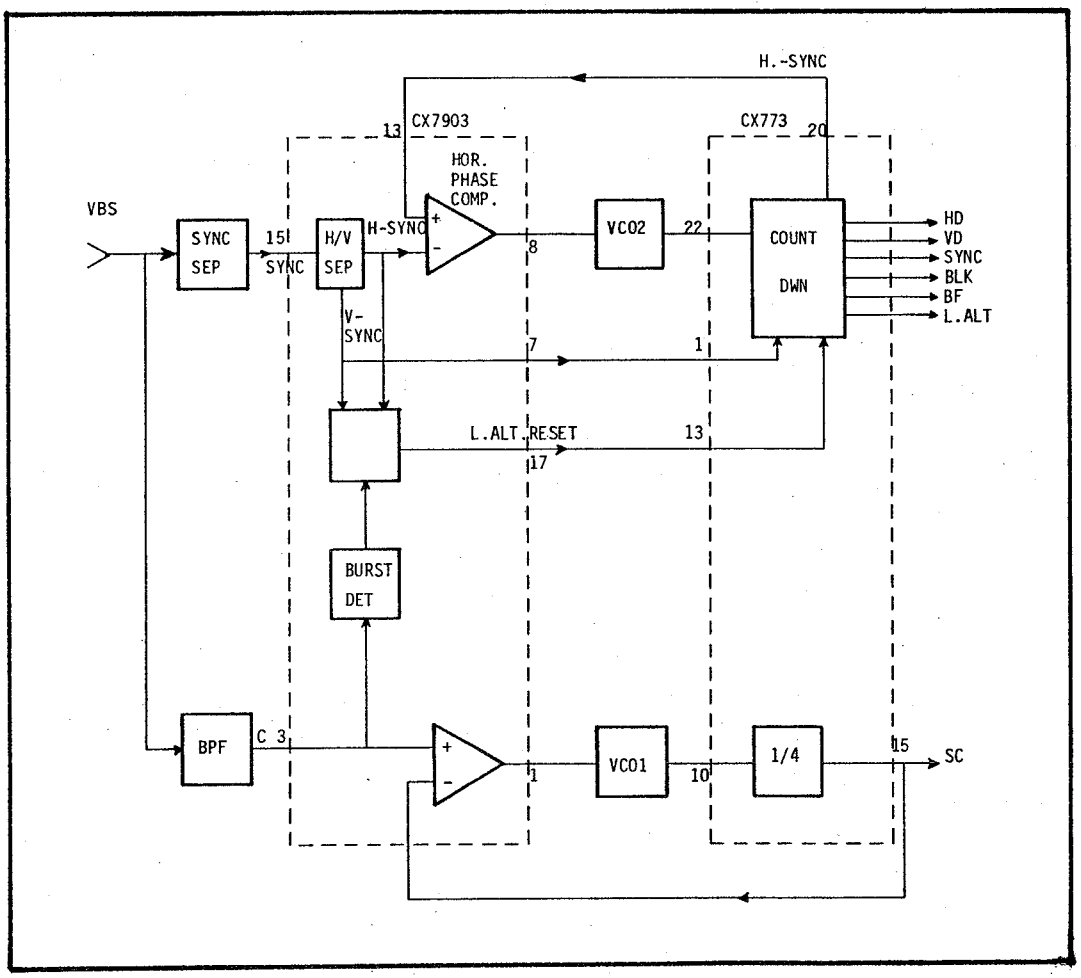


Fig. 3-3. Sync generator in EXTERNAL mode.

The sync separator is of an elaborate design. This is necessary to reduce timing errors and jitter in locked sync. (spec ± 30nsec). Especially because gen-lock from the CCU is also return video and subject to (sudden) APL variations. D1 is a preliminary clamp. Subcarrier is eliminated by trap L3, C4. Q3 is a simple sync separator.

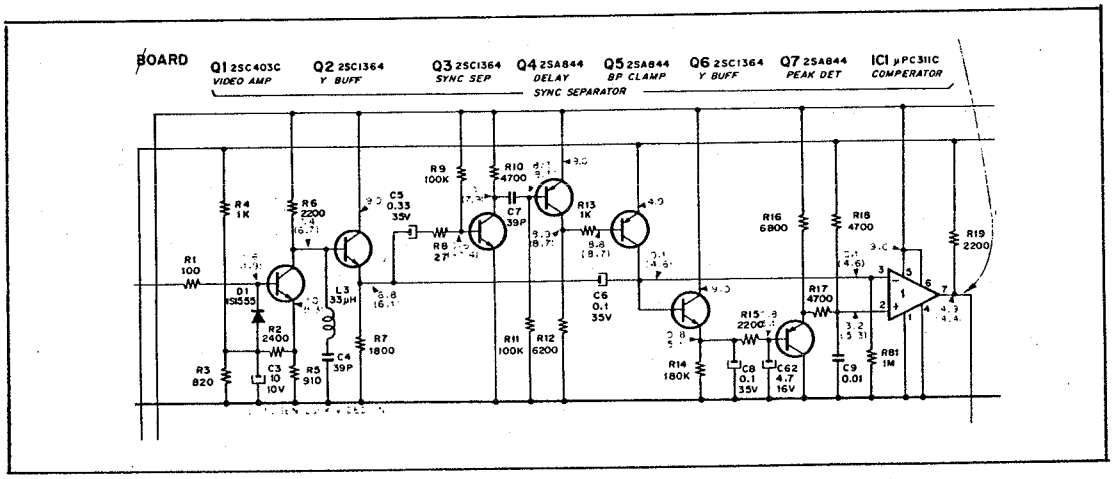


Fig. 3-4. Complete sync separator.

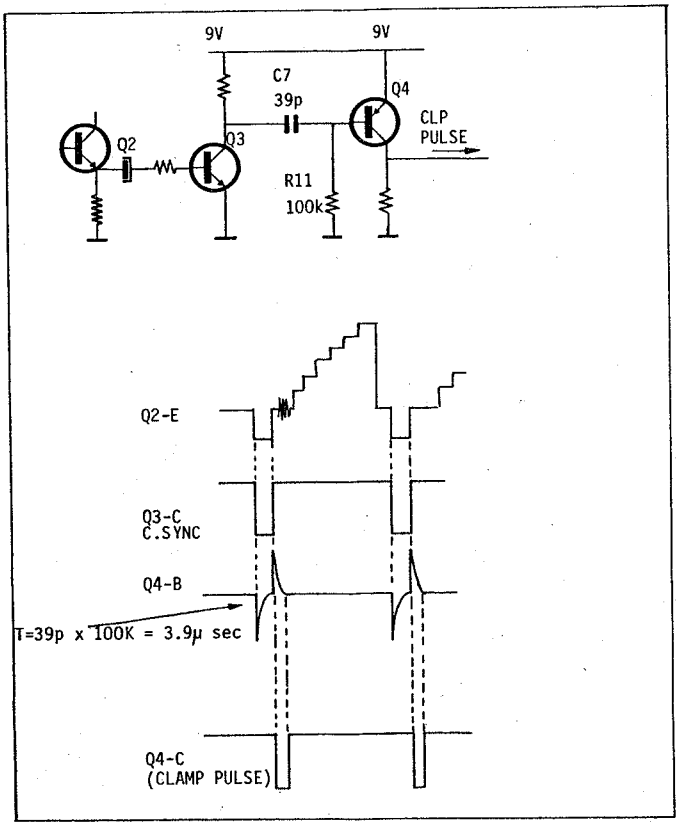


Fig. 3-5. Auxiliary sync separator and differentiator.

The output is differentiated by means of C7,R12 to produce a positive

spike at the end of horizontal sync.

This pulse is shaped with Q4 and then used to clamp the back-porch of the video signal to +5V. Q6 with C8 form a peak detector. PNP transistor Q7 compensates the base-emitter offset of Q6.

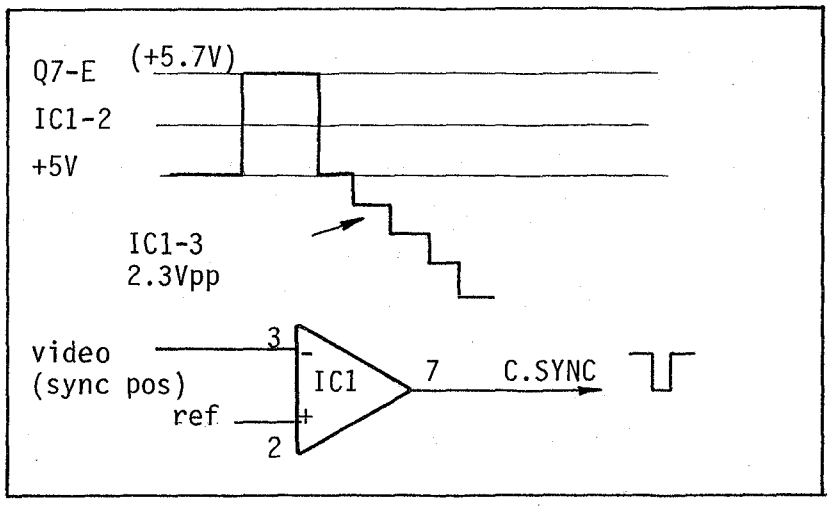


Fig. 3-6. Waveforms at comparator IC1.

The center voltage between sync tip and +5V is obtained by divider R17,18 and compared to clamped video in IC1, μPC311C (fast comparator). This produces a composite sync signal which is fed to genlock IC CX7903.

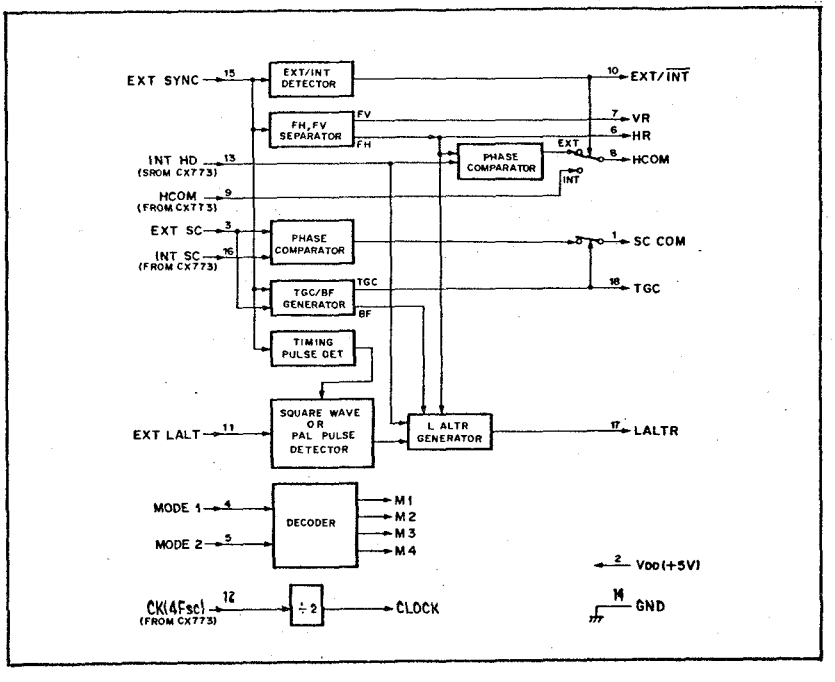


Fig. 3-7. Functional diagram of CX7903.

The presence of (external) composite sync is detected inside CX7903 (and used to switch the H phase error signal). The $\overline{INT}$/EXT is also available at pin 10 and goes to the SC phase error switch IC9 (pins 12,13,14) and to CX773 - pin 16 (EXT).

Hor. and Vert. sync are separated from comp. sync. H. sync. is applied to phase comp. 2.

Chroma is separated by BPF C13,25 and shaped into a square wave by Q10,11. The external (at pin 3) and internal subcarrier (at pin 16) signals are compared in CX7903. The resulting error signal is sampled by burst flag, comes out at pin 1 and goes to the loop filter and VCO1.

H and SC phase adjustment is done by inserting variable delays in the feedback paths to the phase comparators. For horizontal, a TTL one-shot with Schmitt-trigger input SN74LS5221N is used. For subcarrier, special precautions must be taken to stabilise the pulse width.

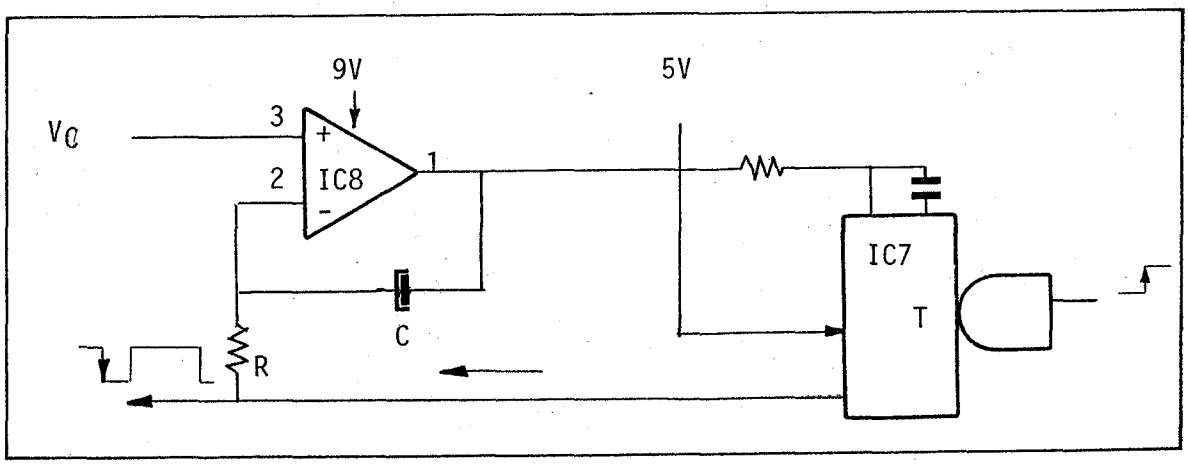


Fig. 3-8. MMV with pulse-width stabilisation.

IC8 functions as an integrator and comparator at the same time. The output (pin 1) will adjust itself automatically until

$$V- = V+$$

$$5V \times \text{duty cycle} = Vc$$

Since the control voltage varies from 0.9 to 3.6V, the duty cycle goes from 0.18 to 0.72 and subcarrier adjustment range is about 200°.

To ensure a 360° control range there is a second MMV with 50% duty cycle and an analog switch.

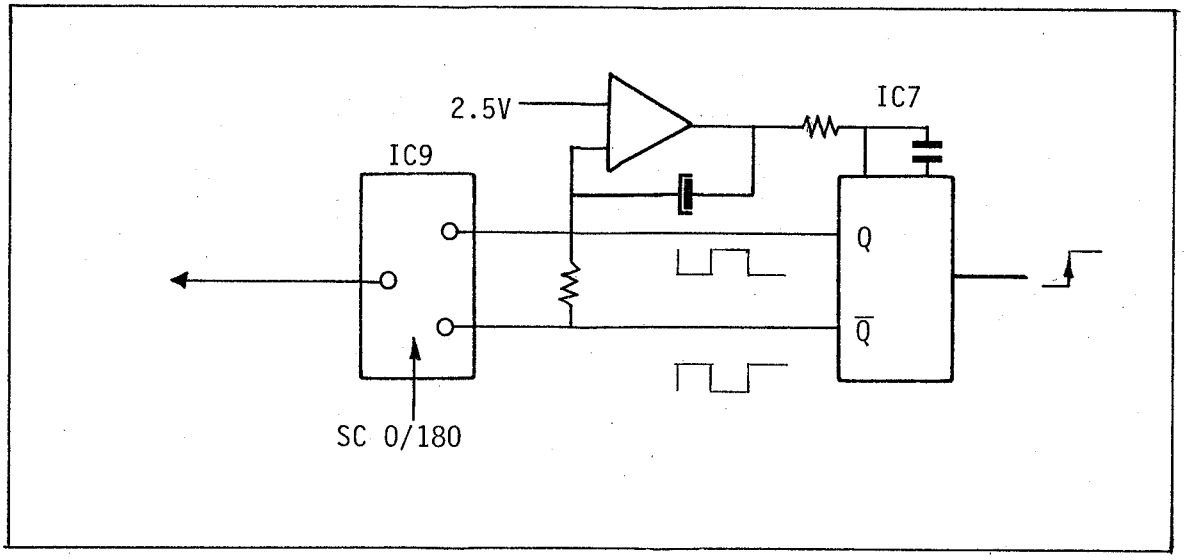


Fig. 3-9. Subcarrier 0°/180° switching.

3-4. SG interface

The shielded case with the SG34 board is mounted on the deflection board DF10. This MCB has some SG signal interface. The reference video as well as the phase control signals have to be switched between local and remote. This is done by means of an analog switch TC4053BP. In CCU mode the gen-lock video comes via the return-video line and the hor/subcarr. phase control signals are PCM-coded on the serial data link.

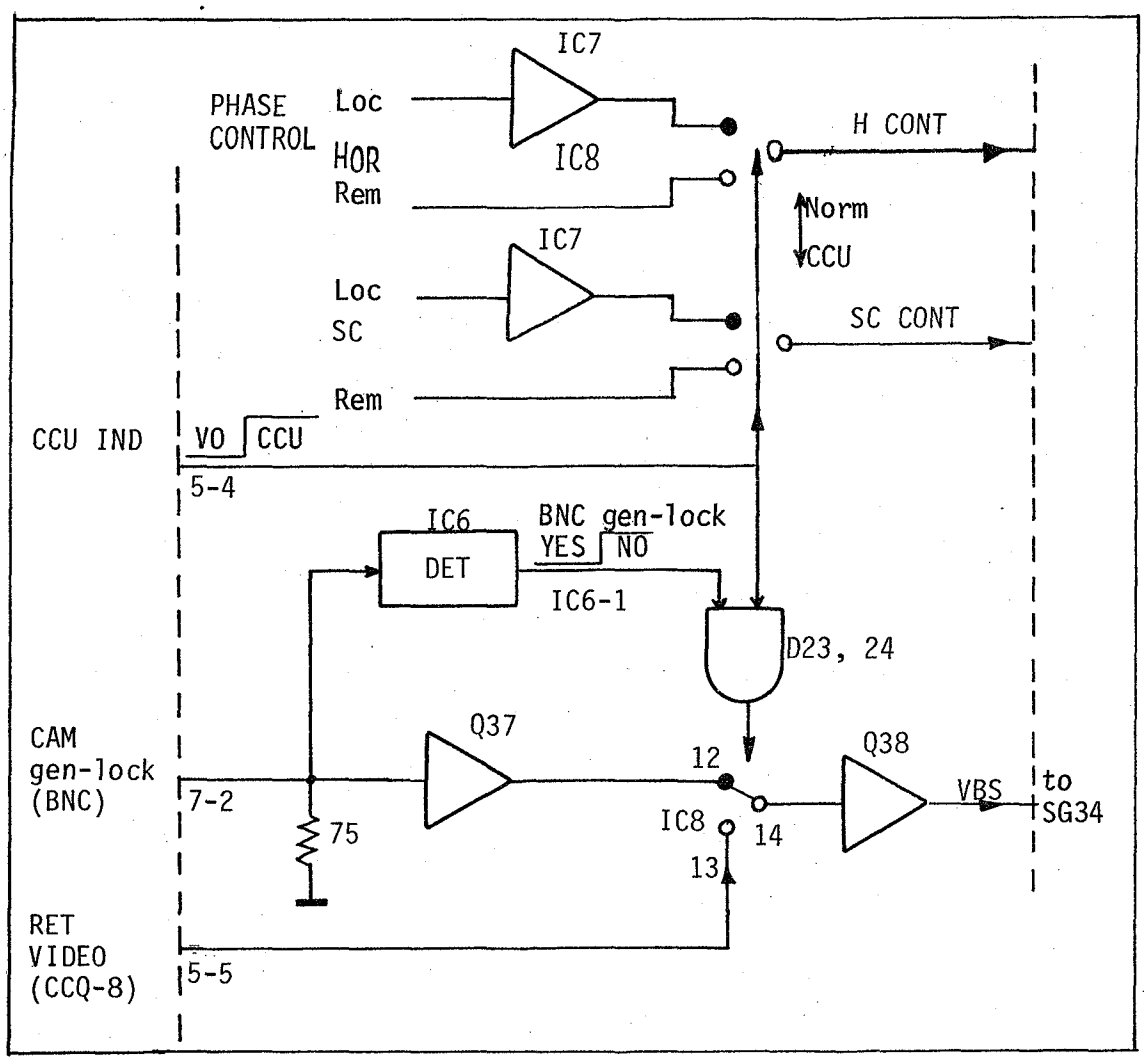


Fig. 3-10. Local/remote reference switching.

Reference signal (VBS) = RETURN VIDEO if CCU mode
and no video present at
camera gen-lock input.

Beside the normal sync pulses, pre-blanking and two different clam pulses are generated. Timing is as follows :

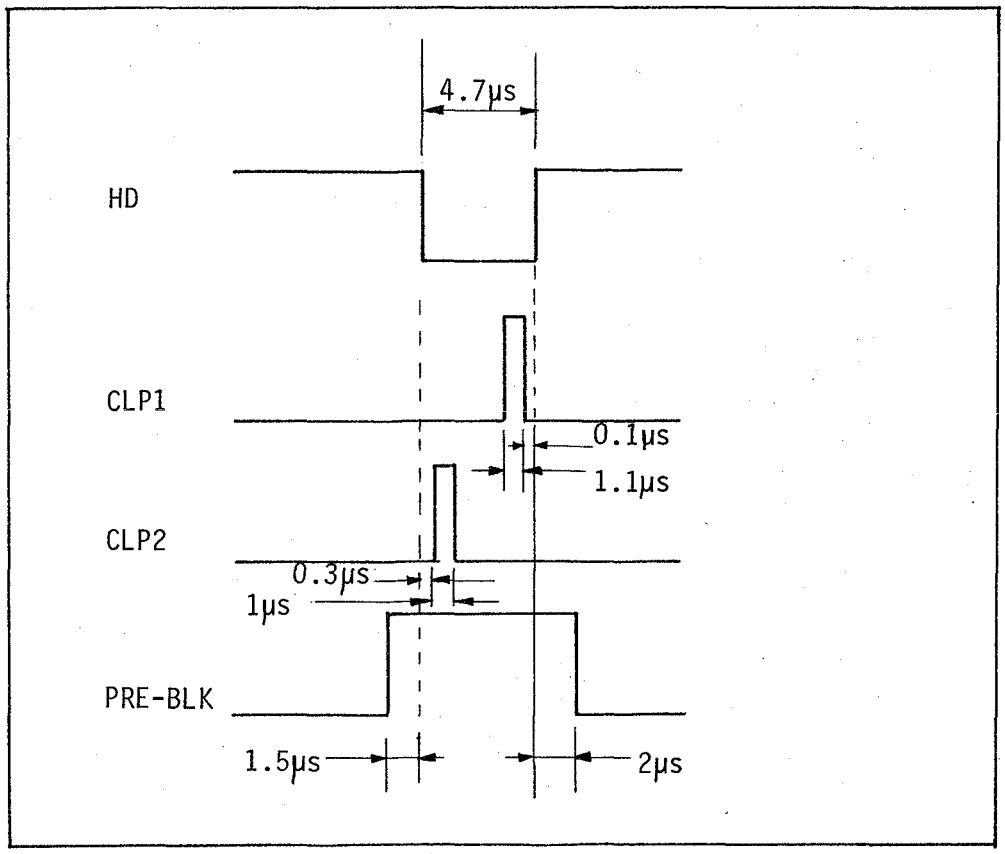


Fig. 3-11. Pre-blanking and clamp pulses.

4. TUBE INTERFACE

This chapter describes all circuits that supply power or signals to the pick-up tube electrodes. All are located on the DF10 board (camera center).

Following functions are involved :

- converter : trigger
  converter
  rectifiers
- deflection : trigger
  separation trafo
  dual sawtooth generator
  centering
- regulators : +5V (from +6.5V)
  -5V (from -6.5V)
  focus (from +6.5V)
  bias light (from +9V)
- others : cathode blanking
  ABO
  quick heat

4-1. Converter

The design is now almost classic, so let us just mention the outputs :

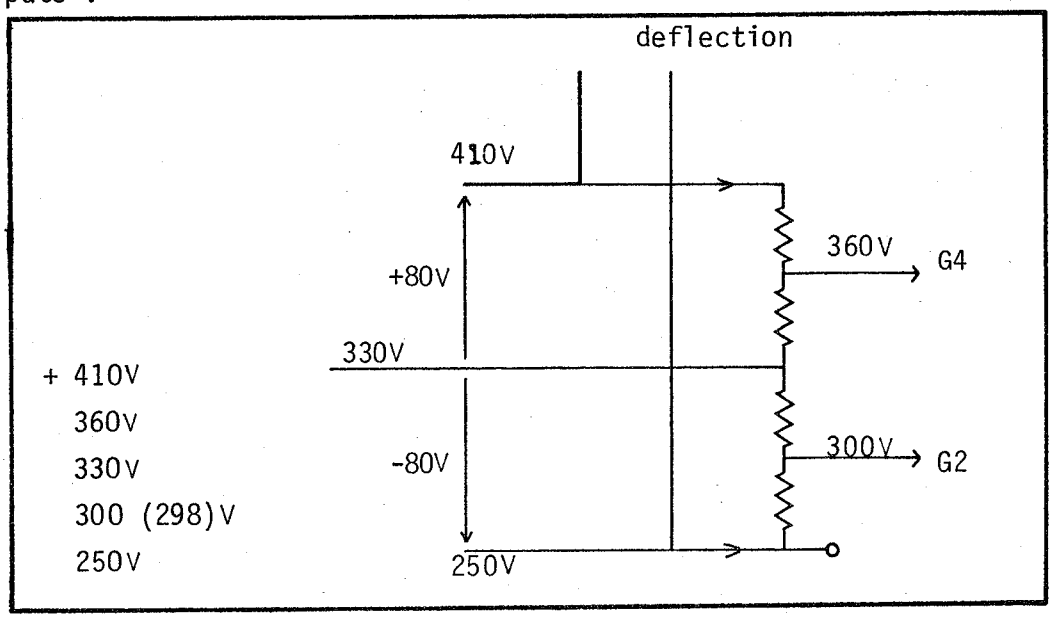


Fig. 4-1. High voltages.

Output	Supply for
100V	target (V_T = 50V)
30V	cathode blanking
	G1 Control grid $V_{G1} \cong$ 3V)
6.5V	heater
	+5 reg
	focus reg (not from +9V)
	(power saving)
-6.5V	-5V reg

Note that the converter is triggered by the L.ALT signal from the sync generator, so that it is always in the same phase relative to PAL-ID. The converter actually serves as buffer between the SG34 and the Trinicon/encoder circuits.

4-2. Deflection

The deflection is electrostatic and two sawtooth voltages of opposite polarity are needed for each scanning direction.

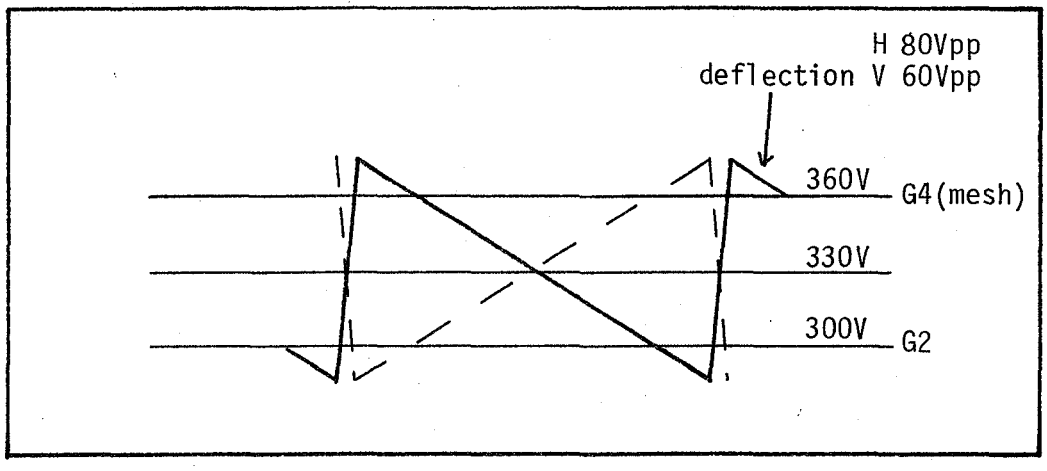


Fig. 4-2. Deflection waveforms.

These waveforms are centered at 330V, which is the average potential inside the pick-up tube between the accelerator grid and the mesh.

The basic generator is shown in Fig. 4-3.

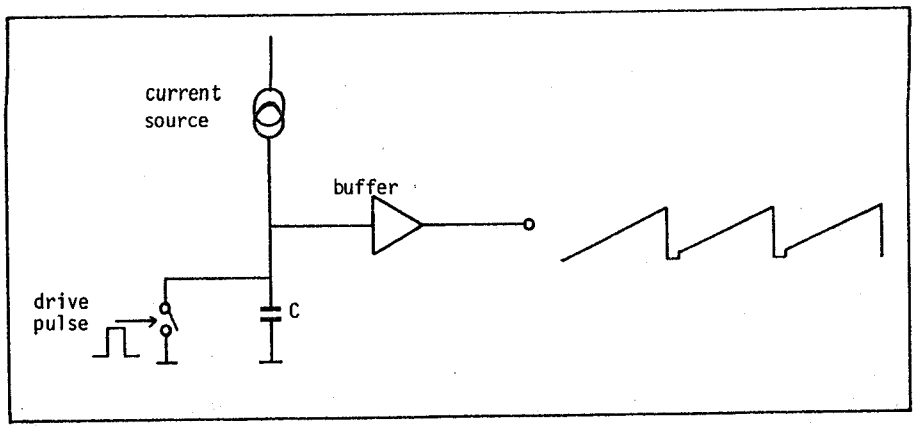


Fig. 4-3. Principle of Sawtooth voltage generation.

The hybrid IC BX369 contains two of these sawtooth generators plus size and centering circuits. The capacitor C is external and is chosen to be 91p for horizontal and 0.047µ for vertical deflection.

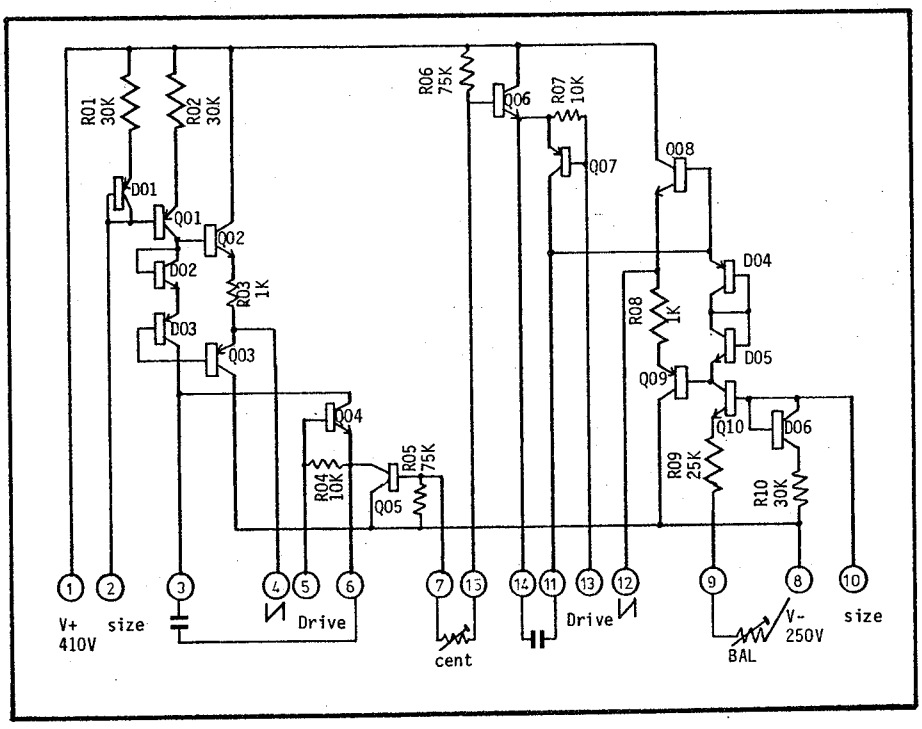


Fig. 4-4. BX369 Sawtooth Voltage Generator IC.

Q1 and R2 form the current source. The capacitor is connected between pins 3 and 6. The ramp resulting at pin 3 is buffered by Q2,3 and is taken out at pin 4. The circuit for the negative going ramp is equivalent. The size potentiometer is connected between pins 2 and 10, and changes the bias to the current sources, varying the rate of voltage build-up. The centering potentiometer is between 7 and 15. Note that the capacitors are not returned to V+ or V- but to a level that is off-set and can be changed with the centering potentiometer.

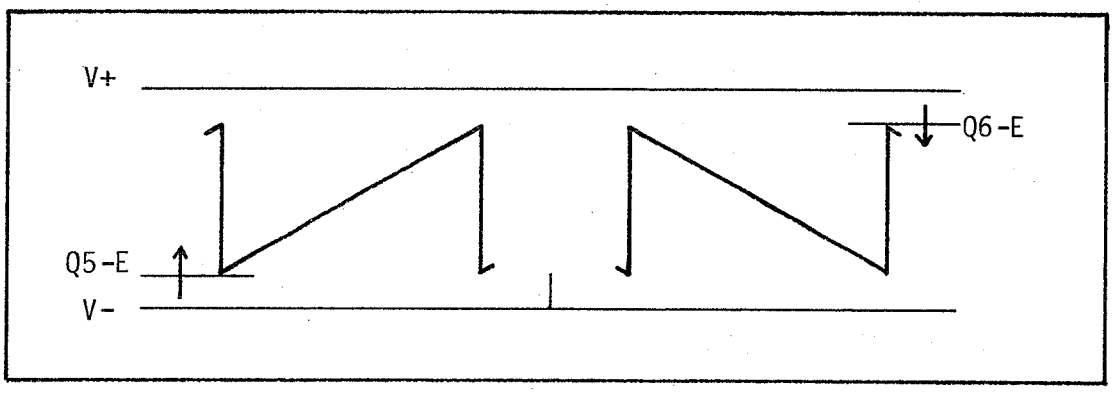


Fig. 4-5. Centering adjustment

4-3. Quick start

Quick start-up is obtained by increasing the initial heater voltage. It now takes about 5 seconds to get a coloured picture on the monitor (against more than 10 for previous DXC cameras). This is a useful feature for intermittent use with a portable VTR, and also reduces the danger of a "sleeping cathode" after long storage.

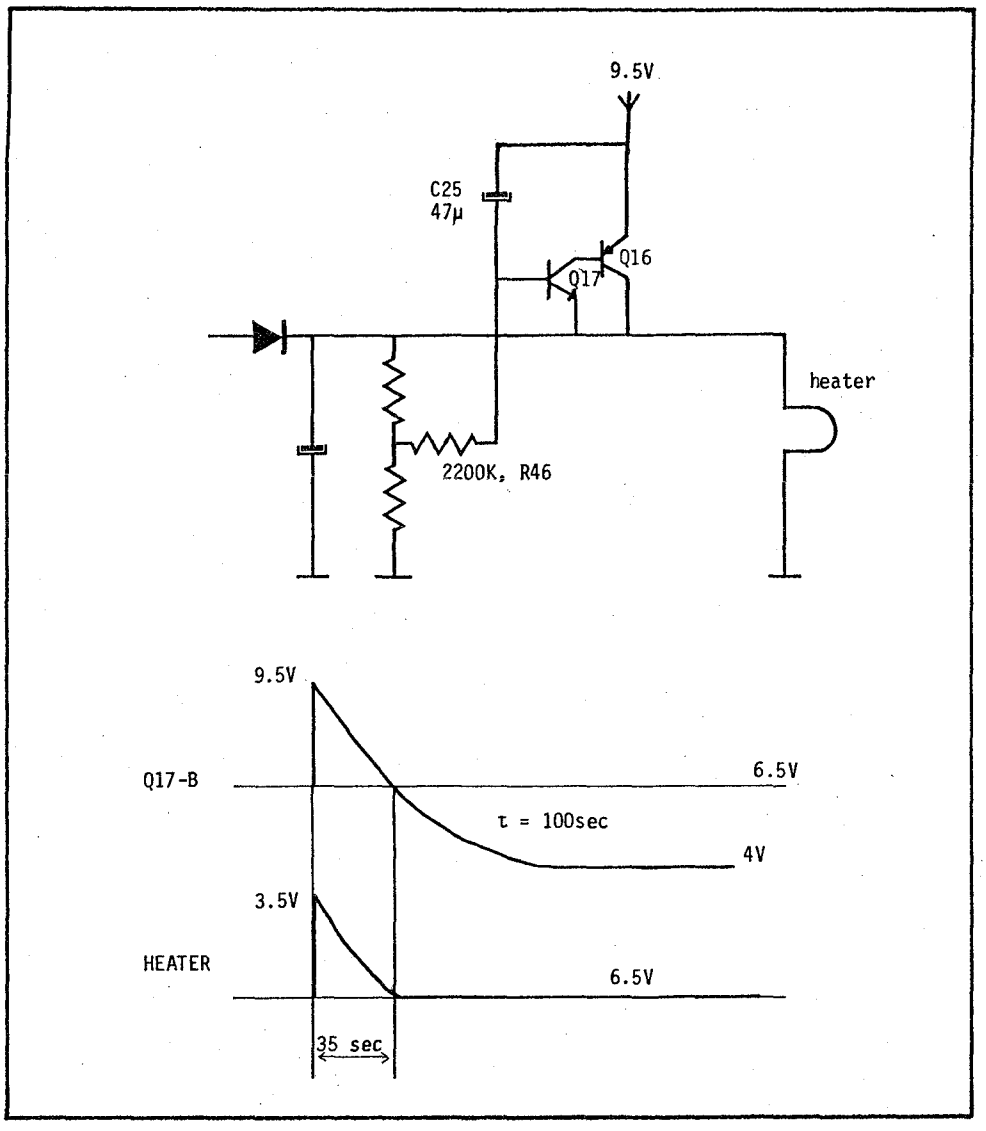


Fig. 4-6. Quick start circuit.

Normally Q17 and 16 are off and heater voltage is 6.5V. But at power on, C25 charges through R46 with a time constant of

$$47.10^{-6} \times 2200.10^{3} \cong 100 \text{ sec}$$

The output follows Q17-base until this one drops below 6.5V. The extra heat-up lasts about 35 seconds.

Since C25 also discharges through R46, it takes some time after switch-off to reach the initial condition. So when turning the camera on a-gain immediately, there is less extra-heating (max. voltage 8V).

4-4. ABO

Camera tubes must often operate with scene contrasts beyond the normal range. When specular highlights (such as the reflections of the sun or a spotlight from chrome surfaces) or a direct view of a light bulb are present in the scene, contrast ratios of 10000 to 1 are involved.

The tube should cope gracefully with the situation : the rest of the picture must not be influenced and there should be no after-effects. This will be the case if the beam current is at least as large as the maximum signal current. If the beam is insufficient to respond to these highlights, the field across the photoconductor will momentarily collapse resulting in target inversion and blooming.
After removal of the highlights it takes several seconds before the target equilibrium value of 0 volts is reached again.
If the highlight travels across the scene the effect resembles the tail of a comet. It is more pronounced with saticon tubes because of the characteristics of the photoconductive layer.

Continuous operation at the very high beam current necessary to respond to the peak signal, regardless of illumination, would result in deteriorated focus and shortened life of the gun cathode.
The "automatic beam optimiser" dynamically changes the beam current to avoid the comet-tail effect. In normal conditions the beam current is constant and adjusted to stabilise up to twice the normal peak signal current.

The ABO circuit takes a sample of the video signal after the pre-amp. The portion of the waveform exceeding a certain level is added to the G1 electrode bias voltage. So when the signal rises, beam is increased automatically.

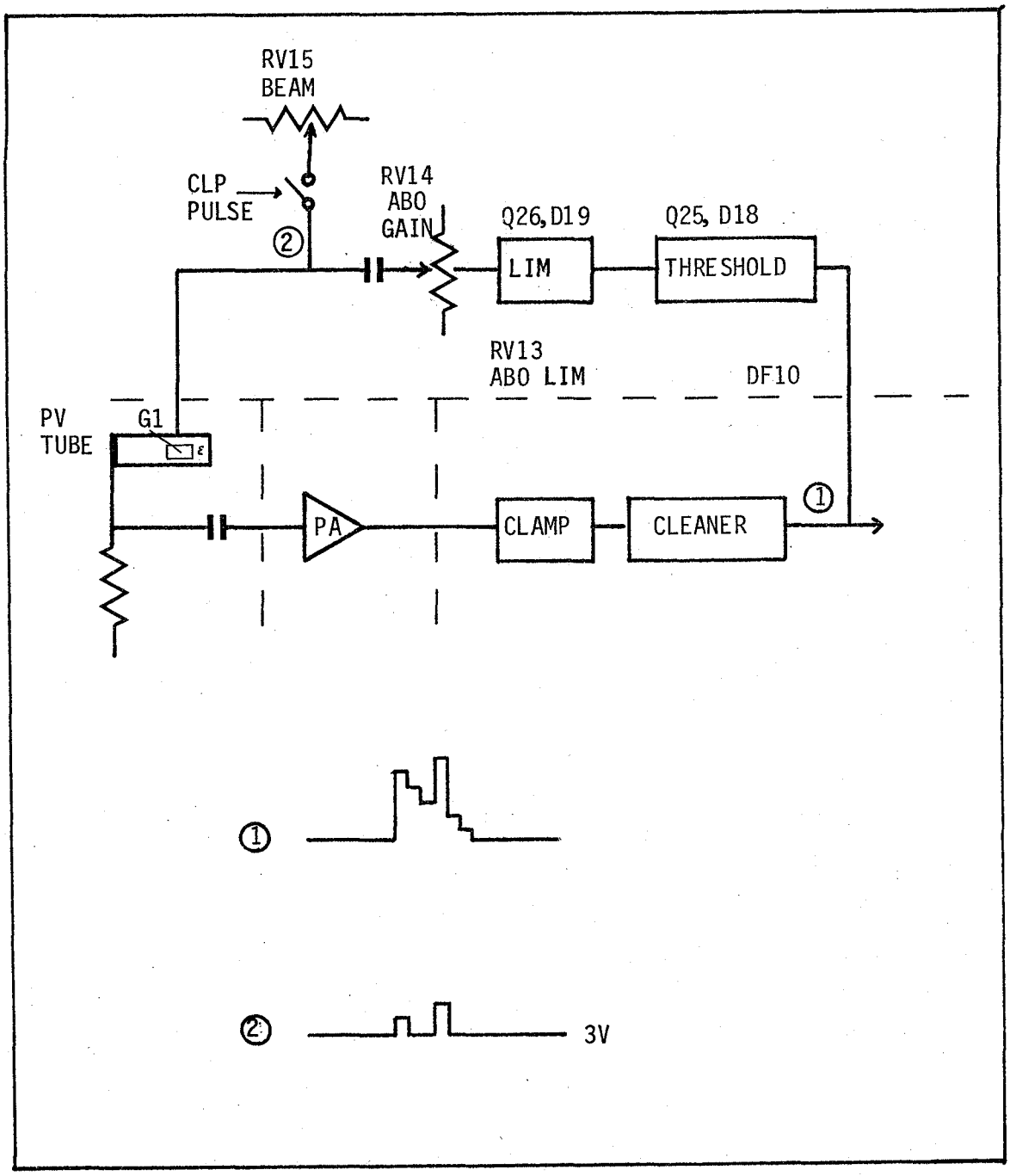


Fig. 4-7. ABO Block diagram

The ABO is adjusted to properly handle highlights up to 6 times normal peak values.
This applies to signal current as well as light intensity since the saticon tube has a nearly linear transfer characteristic

5. THE 2/3" SMF PICK-UP TUBE

5-1. Introduction

Selenium is not a new photoconductor; in fact, it is the oldest known. In 1873 a rod of selenium was being used as a resistor in a piece of equipment for testing the resistance of transatlantic cables as they were being laid. It was observed that the instrument readings varied regularly during the course of a day; these changes were traced to the influence of light on the selenium resistor. Since that time, selenium has been used in a host of light-sensitive devices, including photographic exposure meters and xerographic copying-machine plates.

The first photoconductive vidicons (made by RCA) employed selenium. The high sensitivity, low dark current, and low lag were distinctly advantageous features. The disadvantages were that the tubes suffered from lack of red sensitivity and short life, and the glassy amorphous selenium layer tended to crystallize, even at room temperature, to produce conductive white spots. Unless some method of cooling the tube was employed, this latter characteristic definitely limited tube life. In subsequent development work at RCA, it was found that adding arsenic greatly reduced the tendency for selenium to crystallize. It was also established that adding tellurium would increase the red sensitivity through the entire visible spectrum, and the concept of developing a selenium photoconductor in a heterojunction configuration was explored. Work on the photoconductor was discontinued by RCA before a commercial tube was introduced.

Subsequently, the research laboratory of NHK, the Japanese Broadcasting Corporation, took up the search for a way of making a satisfactory selenium-based photoconductor. After some initial success at NHK, the Central Research Laboratory of Hitachi began to collaborate with them in the development of a practical photoconductor and associated camera tube, with the intent of producing a tube specifically for colour-television cameras. The result of this collaboration was a tube they called the Saticon.

The solution, shown in fig. 5-3, was to incorporate the tellurium in the neighbourhood of the signal plate to achieve good red sensitivity, but far enough away from it to prevent disruption of the barrier and any recrystallization tendencies. The thickness and the concentration of tellurium in the tellurium-bearing layer determine the increase in the red sensitivity. If the tellurium concentration is too high or the tellurium-bearing layer too thick, the recrystallization tendency increases which in turn increases the tendencies for image retention.

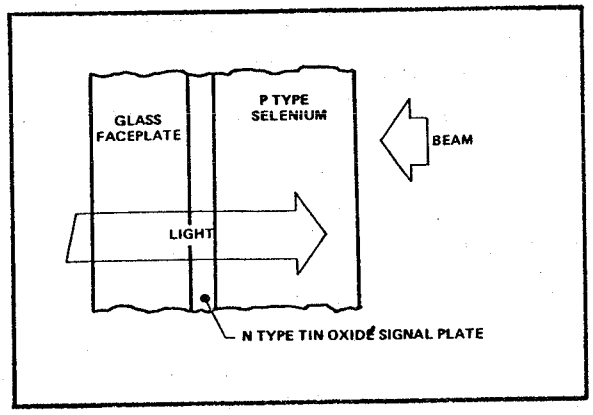


Fig. 5-1. Configuration of a selenium photoconductor in a camera tube

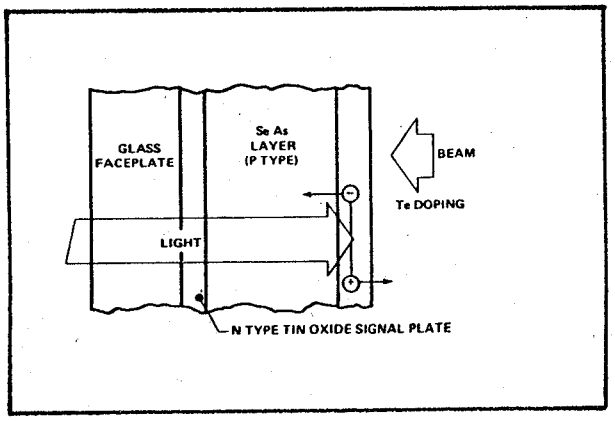


Fig. 5-2. Selenium-arsenic photoconductor doped with tellurium on the scanned side

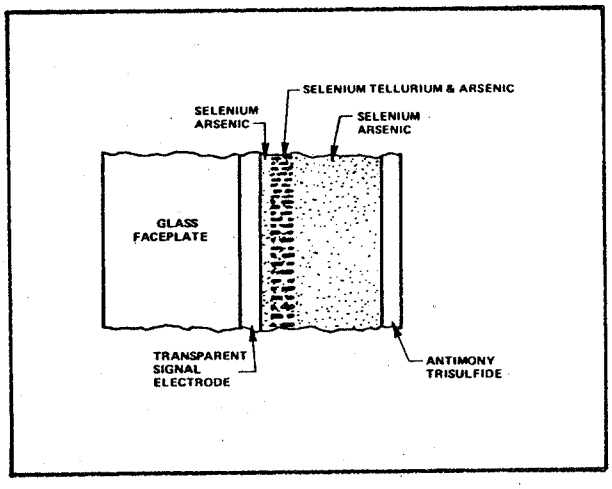


Fig. 5-3. Configuration of the Saticon tube photoconductor

Hence, a balance must be struck between red sensitivity and photoconductor stability and lag.

The thickness of the remainder of the photolayer is also critical because the capacitance of the layer (and thus of the lag) will be high if the layer is thin, while too thick a layer requires too much a target voltage. With a given hole-carrier lifetime and mobility in the selenium-arsenic layer, the electric field must be high enough to pull the carriers through before they are lost by recombination. If the layer is too thick, the target voltage necessary to produce this field is too high and the beam develops "edge crawl" effects near the edges of the picture where the beam seems to oscillate in position and produce a rippled appearance.

The maximum useful target voltage is about 50V, but even at this voltage there could be problems with secondary emission from the surface of the selenium. This secondary emission would introduce instability in the beam or even cause the scanned area to flip over to the "high-velocity" scan mode if the secondary emission becomes greater than unity at this target voltage. A thin, porous layer of antimony trisulphide is deposited on the scanned area as shown in fig 5-4, to reduce this tendency for secondary emission. This layer also enhances the resistance of the photoconductor to the entry of excess beam electrons and produces a reverse-biased junction effect on the scanned surface that reinforces the barrier to excess electrons.

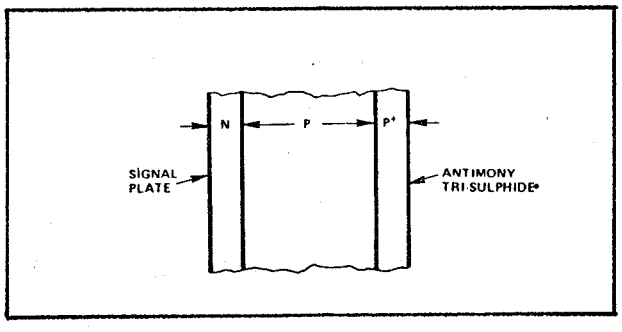


Fig. 5-4. Cross section of Saticon photoconductor showing the electrical-conductivity characteristics

Doping of the photoconductive selenium-arsenic layer with tellurium produces a narrowing of the bandgap in the doped region; this narrowing has an effect on the required field and target voltage. An energy diagram of the photoconductor is shown in fig. 5-5. The field should be high enough so that the saddle caused by the doped region flattens out and allows charge carriers generated in this region to travel through the photoconductor. If the target voltage (or the field) is not high enough, carriers trapped in this saddle cause unwanted image retention and lower sensitivity.

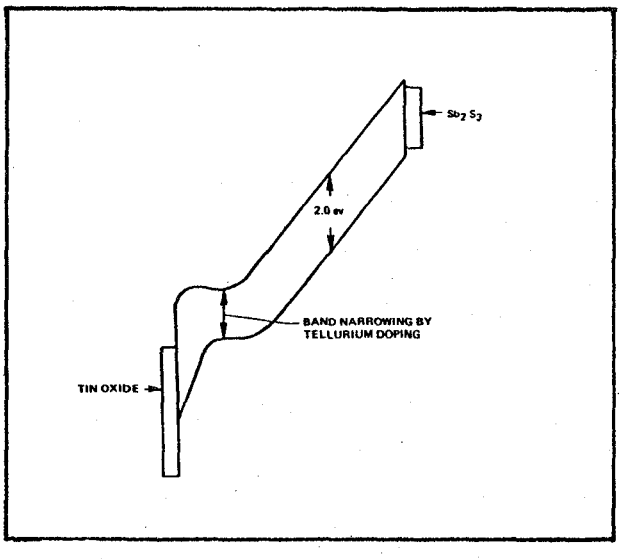


Fig. 5-5. Bandgap and energy diagram of reverse-biased Saticon tube photoconductor

5-4. Photoconductor Performance

The photoconductor that evolved based on the above considerations, the selenium-tellurium-arsenic photoconductor used in the Saticon tube, exhibits the following characteristics.

5-4-1. Sensitivity

In the band of wavelengths, approximating the blue channel of a colour television camera, the photoconductor has nearly 80% quantum efficiency, which is very close to the sensitivity of a lead-oxide photoconductor (one charge carrier per photon is 100% quantum efficiency). The sensitivity decreases through the visible spectrum, as shown in Fig. 5-6. The colour camera green-channel sensitivity of the selenium-arsenic-tellurium photoconductor is 15-20% less than the green-

channel sensitivity of a lead-oxide photoconductor, and the red channel sensitivity is midway between the red-channel sensitivity of a standard and an extended-red lead-oxide photoconductor. At the present time, the red sensitivity of the Saticon photoconductor extends beyond 800nm; the band of light between 700 and 800nm must be excluded from the optical system of a colour camera.

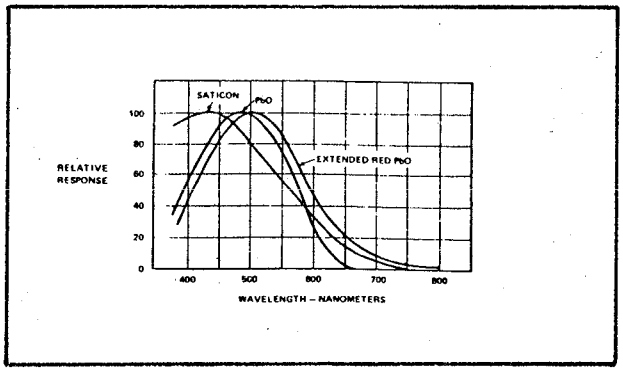


Fig. 5-6. Comparative spectral response

So, the present sensitivity of the selenium-arsenic-tellurium photoconductor is not superior to that of the lead-oxide photoconductor, but it is comparable. In one respect, the photoconductor sensitivity balance is better since there is a better balance between the signal levels of the three channels of a colour camera, compared to when lead-oxide tubes are used in the same camera with tungsten light scene illumination.

The photoconductor has a linear light-transfer characteristic (gamma of unity) over the useful range of signal current.

5-4-2. Dark current and Reflectivity

The dark current in the Saticon tube is extremely low, typically 0.5nA/cm^2, testifying to the efficiency of the reverse-biased junctions. Thus the dark current in a 25-mm Saticon tube with a useful scanned area of approximately 1 cm^2 is 0.5nA; in an 18-mm tube it is 0.25nA.

The optical absorption and reflectance of the photoconductive layer is of particular importance. Glassy selenium is red in colour (i.e. it reflects and transmits red light). The addition of the tellurium reduces this reflectivity and the photoconductor appears nearly black. Measure-

ments of the reflectivity of various typical camera-tube photoconductors are shown in Fig. 5-7.

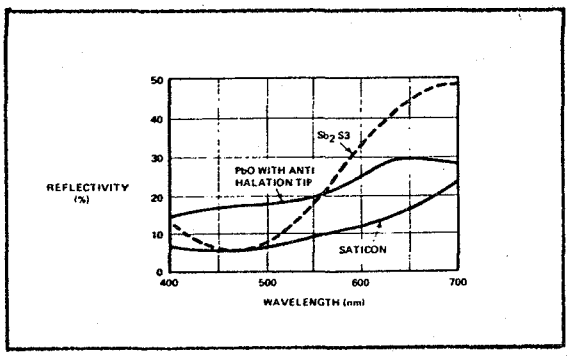


Fig. 5-7. Comparative photoconductor reflectivity

The consequences of this low reflectivity and high absorption are twofold. First, very little light is reflected back into the optical system from the photoconductor. With some camera tubes, particularly with red and green light, an appreciable amount of light is reflected back into the optical system where it appears unwanted in portions of the image and deteriorates the contrast and colour fidelity of lowlights in the picture. It is evident that this reflected light can cause a significant deterioration of image quality, especially in view of the fact that more than 1 or 2% reflectivity from the other optical surfaces of a colour camera optical system is considered unacceptable. The improvements in this characteristic in Saticon tubes are evident in the signal waveforms produced by a high-contrast image transition, and very little flare compensation is needed in the video processing to compensate for light reflected from the photoconductor and scattered over the remainder of the image. The low reflectivity of the Saticon photoconductor, therefore, obviates the need for an antihalation button on the faceplate of this type of tube.

A second benefit accrues from the light-absorbing characteristics and from the homogeneous noncrystalline nature of the Saticon photoconductor. Very little light is dispersed through the photoconductor, a quality that contributes to the good resolution characteristics of this photoconductor as compared to lead-oxide tubes where the crystalline photoconductor disperses red and green light through the photoconductive layer and causes loss in resolution. In Saticon tubes, the resolution is independent of the wavelength of light.

5-4-3. Lag

Lag in a photoconductive camera tube is produced by two factors : trapping effects and storage capacitance. The trapping effects in the photolayer are, in turn, of two types : those that delay the read-out of the charge carriers and those that temporarily lower junction barriers and allow unwanted dark current to flow where the photosurface was previously illuminated. In the Saticon tube, these trapping effects are negligible, and the lag is caused primarily by the second factor - the storage capacitance of the photolayer in series with the effective beam resistance. The storage capacitance of the Saticon photoconductor is higher than of lead-osice photoconductive tubes. This higher capacitance in itself could make the Saticon tube noncompetitive if means did not exist for reducing the resulting lag.

Means do exist, however, and the first and most effective of them is the use of bias lighting. Bias lighting is the technique of putting uniform light on the photoconductor to bring the zero-signal (picture blacks) charge voltage up to some voltage that is nearly as high as the velocity spread of the electrons in the scanning beam. This spreading, expressed in electron volts, represents an effective beam resistance. It was discovered quite accidentally in 1967 that this method of operating a tube (inserting a "dc" illumination level on top of the optical image on the tube and later electrically subtracting this uniform signal or black level pedestal from the signal) is an effective and acceptable method of reducing the lag of a photoconductor when the lag is primarily the result of the storage capacitance of the photolayer. Most television cameras with lead-oxide or Saticon camera tubes now employ this technique. Bias lighting is particularly effective used with Saticon tubes because the photoconductor sensitivity is uniform. The use of uniform bias lighting does not introduce unwanted black-level nonuniformities.
In the 18-mm Saticon tube, another means is used to further reduce the lag, namely the low-beam-impedance gun as will be explained later.

5-4-4. Uniformity and Stability

Other properties of the photoconductor satisfy some of the other developmental objectives. The Saticon photoconductor is a glassy impervious layer that can be exposed to air, sealed to a tube by a cold indium pressure-sealing technique, and even pretested for electrical characteristics. Thus the photoconductor can be made very uniform in thickness since it does not have to be fabricated within the confines of a small bulb, and a large number of faceplates can be processed at one time. Fabricating it with uniform thickness contributes to the Saticon's highly uniform sensitivity over the scanned area; making many faceplates at a time contributes to similar characteristics from tube to tube and makes possible the selection of only those photoconductor lots that meet the desired performance characteristics.

The glassy layer also produces unusual stability of the electrical characteristics with time. It is impervious to doping by gases generated within the tube, and it is not subject to deterioration or change caused by electrolysis effects when current is drawn through the photoconductor. These effects can and do change the characteristics of the porous photoconductive layers of both lead-oxide and antimony trisulfide tubes as they are used or stored.

The Saticon-tube photolayer is a material that is stable over a wide temperature range and that also maintains, practically constant, all of the important performance characteristics such as lag, resolution, sensitivity and resistance to image retention over this temperature range. The tube is rated to operate from 30°C (-22°F) to +50°C (122°F) and can operate for short periods of time at temperatures as high as 65°C (149°F). It appears that operation at high temperatures within this range does not shorten the life of the tube, as is the case with lead oxide.

Another beneficial characteristic of the Saticon photoconductor manufacturing process is the ability to make the tube reasonably defect-free (from spots etc.). The photoconductor is also relativily resistant to damage that can cause spots after it is manufactured, unlike the relatively fragile antimony trisulfide layer.

The occurence of any defects or spots during operation is indeed a rare occurrence.

If the camera is uncapped during stand-by - i.e. when the camera (or the beam) is turned off, any stationary image focused on the photoconductor can be "burned in". However, the tube is resistant to image burn-in for many minutes of stationary exposure when the beam is turned on and the field is maintained across the photoconductor.

5-4-5. Gun design

The performance of the Saticon tube in a colour camera is determined in great part by the design of the electron gun. The foremost innovation in gun design is the low-lag capability incorporated in the gun used in the 18-mm tube. This gun reduces the lag of the tube by reducing the beam resistance. A word is necessary on the source of the effective beam resistance. In any vidicon tube, the beam lands on the target with low velocity. In the absence of a positive charge, the beam slows to zero velocity and actually turns around and does not land on the target. When a positive charge is encountered, electrons land on the charged area until the voltage approaches zero, when the remainder of the electrons are repelled. The electrons in the beam do not have the same energy or velocity nor are they all directed perpendicularly toward the target. A typical plot of the current collected from a beam as the collector voltage is increased from a negative to a positive potential is shown in Fig. 5-8.

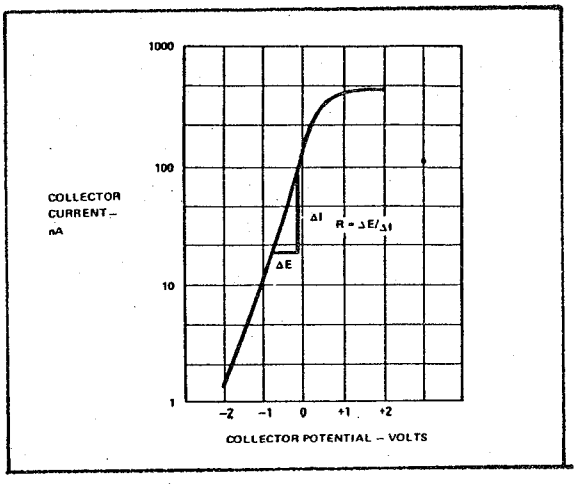


Fig. 5-8. Current/voltage plot of beam current collected from a vidicon-type gun

5-4-6. Use of Bias Lighting

The use of bias lighting has proven to be a universally accepted method of reducing the lag of television camera tubes where the lag is determined primarily by the beam resistance and the target capacitance. Figure 5-12 illustrates the improvement in lag as the bias-lighting signal level is raised on the 18-mm Saticon tube. The amount of bias lighting that can be used is limited by the uniformity of the background signal produced, which is determined primarily by the uniformity of the bias lighting. When the cameras are operated at very low light levels and low signal levels (approximately 30 nA in the lowes signal channel), the practical bias-current limitation is 5-10 nA.

Even more significant in the use of bias lighting is the improvement in signal build-up. In the absence of light, there are yet a few beam electrons that have enough energy to drive a low-dark-current photoconductor considerably below 0V. When light is encountered, the target must be charged up to 0V before the beam can begin to develop significant signal from the target. Figure 5-13 illustrates the build-up improvements as a function of bias lighting. It is easily seen that only a modest amount of bias-lighting current is needed to improve the build-up characteristics. Poor build-up of a signal in a colour camera is noted as changes in the colour or brightness of the leading edge of an object moving against a dark background.

Contrary to what might be expected, the use of bias lighting does not distort the tonal values of the picture developed by a linear photoconductor. Bias light adds to the dc signal-level an amount that can be subtracted out by black-level adjustments in the video processing amplifier.

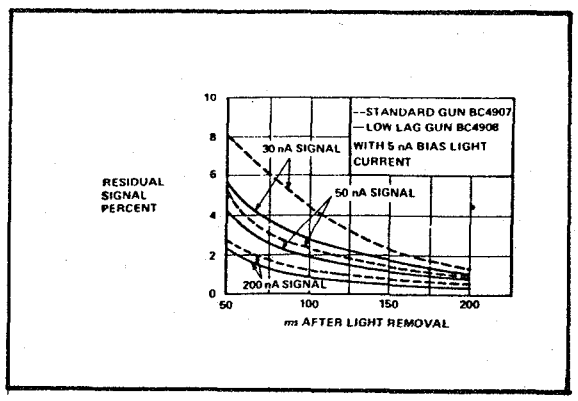


Fig. 5-12. Reduction in lag obtained by the use of the low-lag-gun.

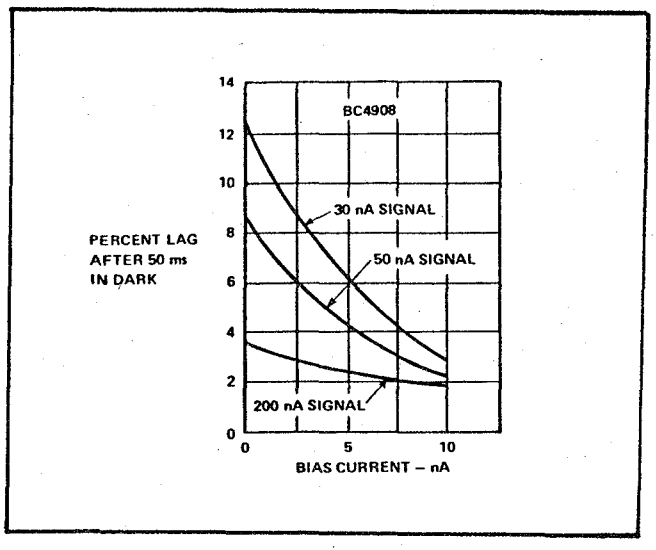


Fig. 5-13. Lag reduction with bias lighting

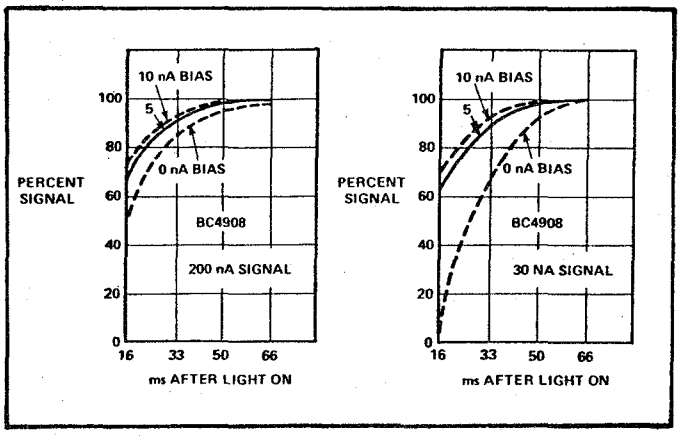


Fig. 5-14. Improvement of build-up with bias lighting

5-4-7. Resolution

The size of the tube was determined by the resolution available. The high resistivity of the photoconductor and the lack of optical dispersion produced a target capable of excellent resolution with a small image size (6.6 x 8.8 mm); the electron gun was designed to maintain this resolution. The result is a tube with a resolution superior to that of 18- and 25-mm lead-oxide tubes and one that begins to rival the resolution of the 30-mm lead-oxide tube.

Figure 5-14 shows amplitude-response curves for the camera tubes discussed in this paper. Measurements were made in the same piece of test equipment with the same test methods.

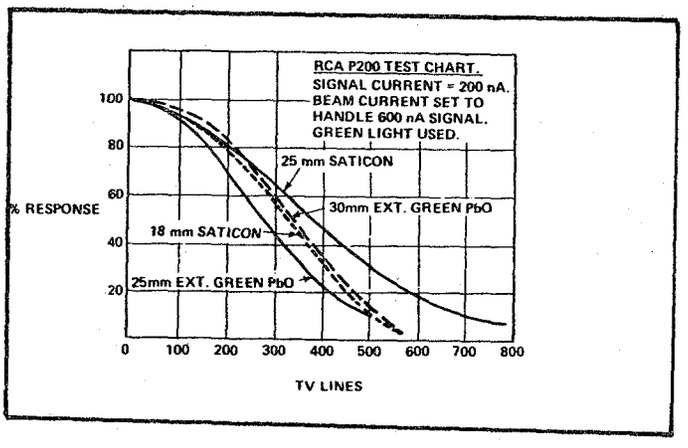


Fig. 5-15. Relative amplitude-response curves of camera tubes used in broadcast service

It should be noted that the amplitude-response curves are not as high as those quoted by other tube manufacturers because the measurements were made using the RCA P 200 slantline test chart, which eliminates the video amplifier frequency-response characteristics as a major factor in the measurement. The numbers developed by this test are generally more pessimistic than those developed by other techniques, but they are very reproducible from one test unit to another.

5-4-8. Size and Sensitivity

The 18-mm tube also has less target shunt capacitance to ground than a 25-mm or 30-mm tube, a factor that contributes to lower noise in the video signal. The smaller size of the tube does not affect the camera sensitivity; the tube produces the same signal output from the same number of lumens of light as does a larger tube. When the depth

of focus and angle of view of an optical system using this smaller tube is identical to that of a camera using a larger tube, the illumination (in lumens) of both tubes will be identical; therefore, there is no sacrifice in sensitivity in employing the smaller, lighter-weight tube. An added bonus to using the smaller-size tube is the lower lag that results from the lower storage capacitance of the smaller area of photoconductor, typically 1400pF in the 18-mm tube.

5-5. Summary of Objectives and Means

In summary, the performance goals for a small high-performance colour television camera tube are achieved in the Saticon by virtue of inherent characteristics of the photoconductor and enlightened design techniques. In particular, the objective of high resolution was attained by adapting an amorphous or glassy photoconductor with low-light dispersion and high-resistivity characteristics and combining this with the use of a well designed electron gun. Low lag was achieved by employing bias lighting, a no-crossover diode gun, and a thick transport layer on the small-area photoconductor (made possible by the high resolution of the photoconductor). Sensitivity and spectral response depend on a highly absorbing photoconductor doped with tellurium to enhance red sensitivity, good hole transport characteristics, and a heterojunction structure that permits high target voltage with low dark current.

The objective of a long life for the Saticon tube was met by employing a glassy-type photoconductor that is impervious to the tube atmosphere, arsenic doping of selenium to reduce the tendency for selenium to crystallize, and a photoconductor that does not out-gas and contaminate the cathode. Freedom from blemishes was achieved by using special substrate processing techniques and a tough, dense photoconductor that is not easily damaged. A competitive camera tube should be resistant to image burns, which implies for the Saticon not only low trapping in the photoconductor as a result of material purity and control but also an electronic design of the photoconductor that maintains adequate electric field throughout the photoconductor in spite of discrete doping sites. The Saticon is designed to be useful over a wide temperature range, and this required doping

of the selenium with arsenic and treatment of the substrate to avoid nucleation sites. (The high resistivity of the selenium maintains resolution at higher temperatures, and proper deposition conditions prevent fracturing to the photoconductive layer under thermal stress.)

As a result of these objectives, the Saticon tube has become a serious challenger to the lead-oxide camera tube in broadcast cameras. The Saticon tube can replace 18-mm (2/3"in) and 25-mm (1-in) lead-oxide tubes in many cameras that are presently in use. The low lag good spectral response and high resolution make the 18-mm tube a suitable replacement for vidicons in approximately designed trinicon cameras. (Since the Saticon layer is sensitive to burn-in when no field is applied, care should be taken to cap the camera lens after use.)

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Comparison S_b S_2 and Saticon trinicon tubes

	2/3" MF	2/3" SMF
used in	DXC-1640P	DXC-1800P
HEATER	6,3 V	6,3 V
GYN SYSTEM	NORMAL	DIODE
CATHODE	0V	0V
G1 CONTROL	-50V	+ 3V
G2 ACCEL	400V	300V
G4 MESH	450V	360V
INT. BIAS LIGHT	NO	YES
FOCUSING	MAG	MAG
	150mA	120mA
TARGET	S_b S_2	SATICON
	10-20V	50V

6. VIDEO AMPLIFIER

6-1. Pre-amp

The pre-amp circuit of the DXC-1800P is analogous to that in previous cameras but has been improved with respect to noise. An FET 2SK152-3 is used. The S/N ratio of the pre-amp alone is 50dB and that of the camera 48dB at 0dB gain/F4 and 2000 lux.

The V line-crawl adjust potentiometer has been removed from the pre-amp circuit to eliminate the risk of bad contacts. Y line-crawl is cancelled using the 1H- delayed Y-signal from the vertical aperture corrector.

6-2. Iris control

The iris has three modes of operation :

- mechanical
- auto
- remote.

"Mechanical" means that the iris control ring is rotated by hand in position C through 1.4. The system is automatic when the iris ring on the camera (and the switch on the control unit) are in position "auto". In this mode the iris closes when power is switched off. With the ring in A the iris can be controlled manually from the CCU. When the ring is turned to AL, the iris set automatically or remotely is held. The iris drive uses a meter system with a control CN6-3(+)/5(-) and a damper winding (CN6-1/4).

In auto-mode (Q63 off) the reference voltage is compared to rectified video.

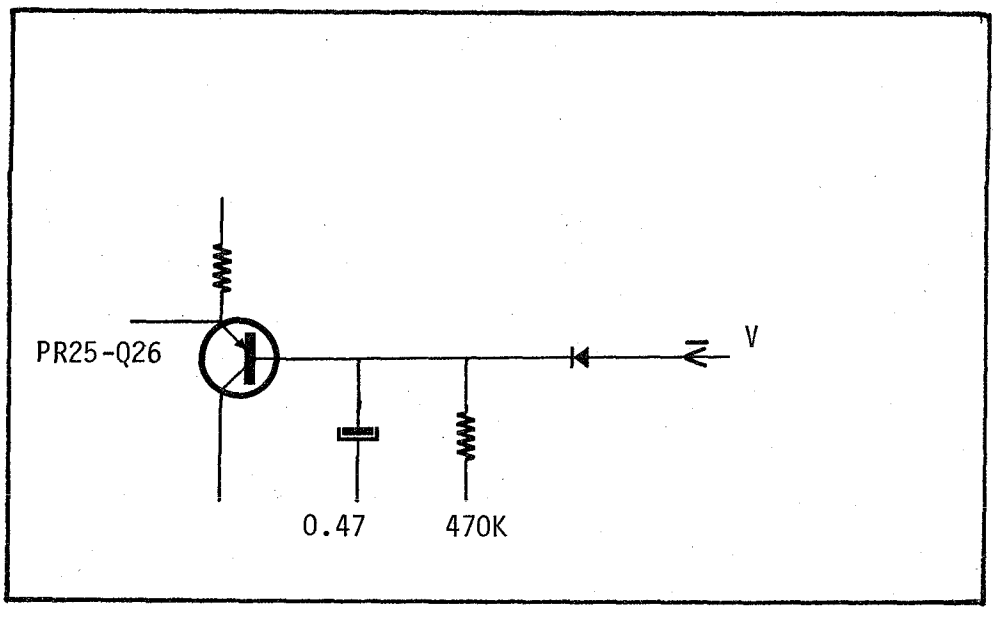


Fig. 6-1. Video detector for the auto-iris system.

The detector has a rather short time-constant of 0.22sec. but the iris movement is damped and therefore slower than the AGC.

In manual mode, a control voltage between 0 and 5V is compared to the iris position signal, which has following value :

5V	iris closed
4V	iris F 1.4

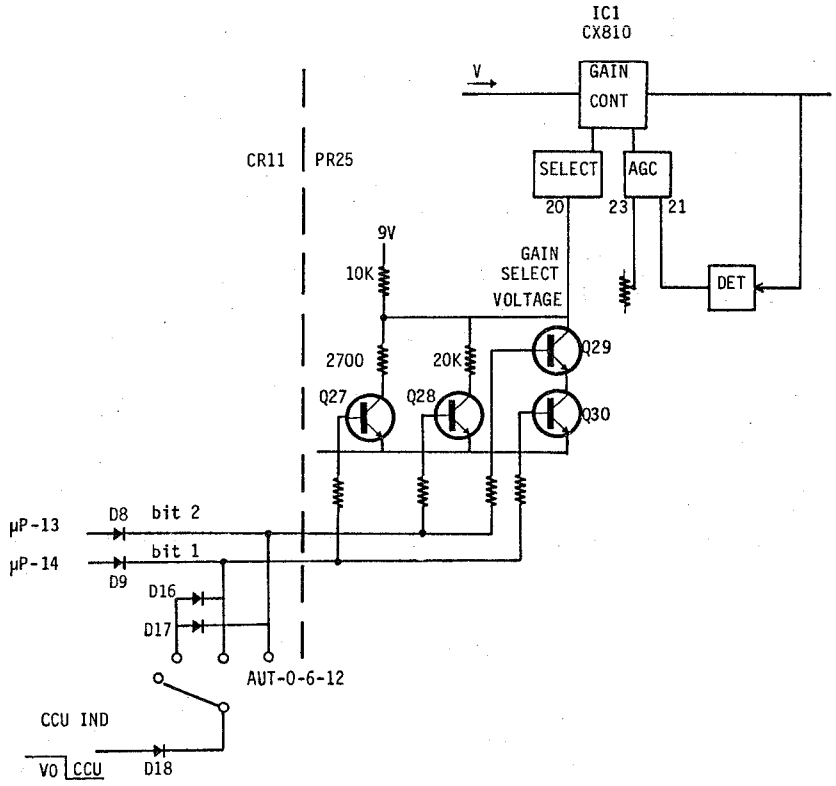
The center of the manual adjustment range is set with RV28 (DC shift of control voltage).

6-3. Gain control

Can be automatic or manual.
In manual mode, there is no continuous adjustment but three fixed steps : 0, +6 and +12dB. This is a more professional approach and provides control of signal-to-noise ratio.
In standard conditions with 0dB gain, the peak video level at PR25-TP1 is 200mV, and at the output 1V. The S/N ratio is now 48dB. Other lighting conditions or lens aperture that give 1Vpp at the output also provide a 48dB S/N ratio.

gain	$S/_N$	lighting at F4	lighting F 1.4
0 dB	48 dB	2.300 lux	300 lux
6 dB	41 dB	900 lux	125 lux
12 dB	33 dB	300 lux	40 lux

Fig. 6-2. S/N ratio and sensitivity at 0dB/6dB/12dB gain.



GAIN BIT 1	GAIN BIT 2	GAIN SELECT VOLTAGE	GAIN dB
1	1	0V	0
1	0	2V	6
/	/	4V	9
0	1	6V	12
0	0	8V	AUTO

Fig. 6-3. Gain selection.

The gain is selected by two logic signals that are set remotely via the microprocessor, or by the camera gain switch. The table is self-explanatory.

In the auto mode, the video signal is rectified by a combination peak-average detector.

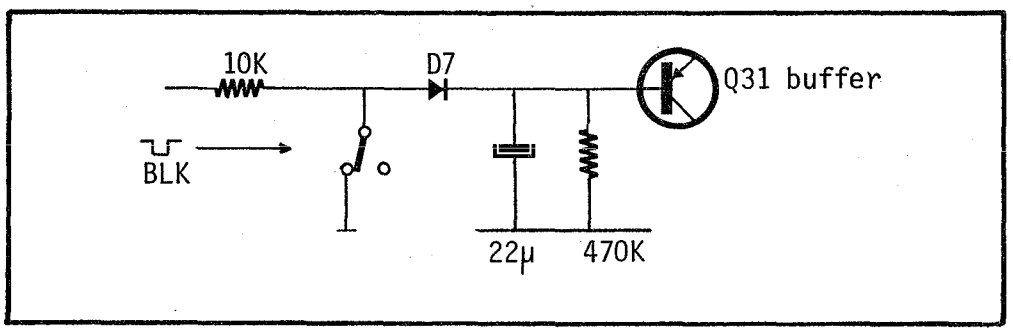


Fig. 6-4. Video-detector for gain control

The negative going time constant is 22 x 470 = 10,3 sec. This relates to the AGC response time when scene brightness decreases. In the opposite direction, response is practically instantaneous.

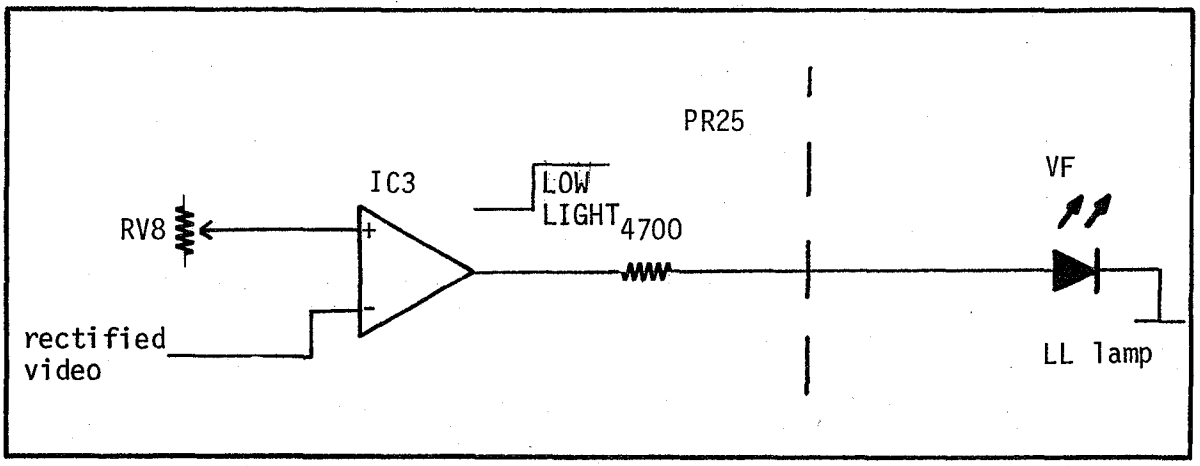


Fig. 6-5. Low-light indicator.

The low-light detector threshold is set in the factory at

$$\frac{250mV}{700mV} = 35\%$$

7. Y PROCESSING

This part of the circuit is similar to the signal process in a B/W camera, and has following functions :

low-pass-filter
equalising delay
image enhancer hor./vert.
line crawl cancel
gamma correction
pedestal set, blanking
white clip
auto-black-level (ABL)

The LPF separates Y from the trinicon signal. A delay is included to compensate the group delay of the chroma channel.

7-1. Image enhancer

Principle :
Image enhancement (=aperture correction=crispening) consists of adding the first to, or subtracting the second derivative from the original signal to improve the rise-time.

The result is an apparent increase of sharpness although the modulation depth as a function of frequency is not altered.

1st order correction : $f_{corr} = f + kf'$
2nd order correction : $f_{corr} = f - kf''$

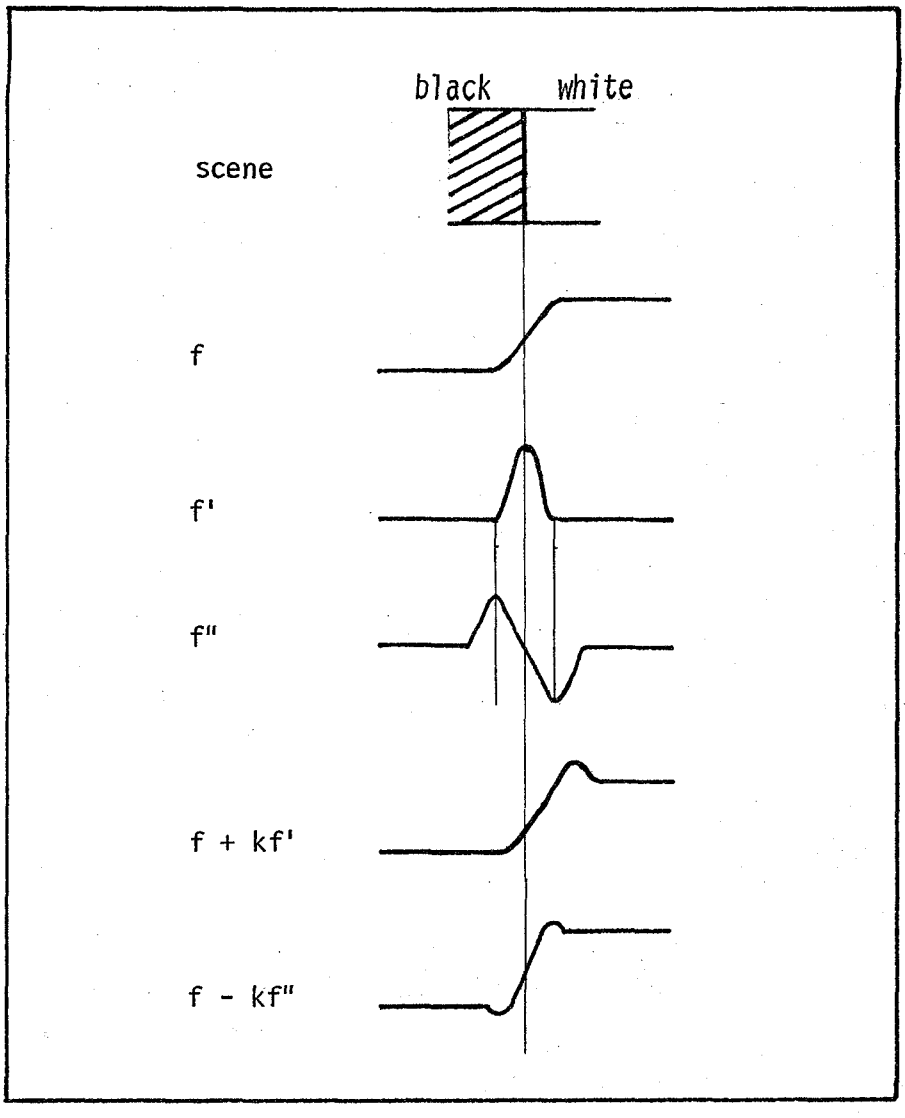


Fig. 7-1. Principle of aperture correction

2nd order correction is better because it produces less distortion (overshoot) for the same amount of correction.

In practical circuits the derivatives are approximated by differences :

$f'(t)$ approx. $= f(t + \Delta) - f(t)$
$f''(t)$ approx. $= f(t - \Delta) + f(t - \Delta) - 2f(t)$.

The delays required are approx. 200nsec for hor. and 64μs for vert. correction.

The block diagrams of aperture correction are as follows :

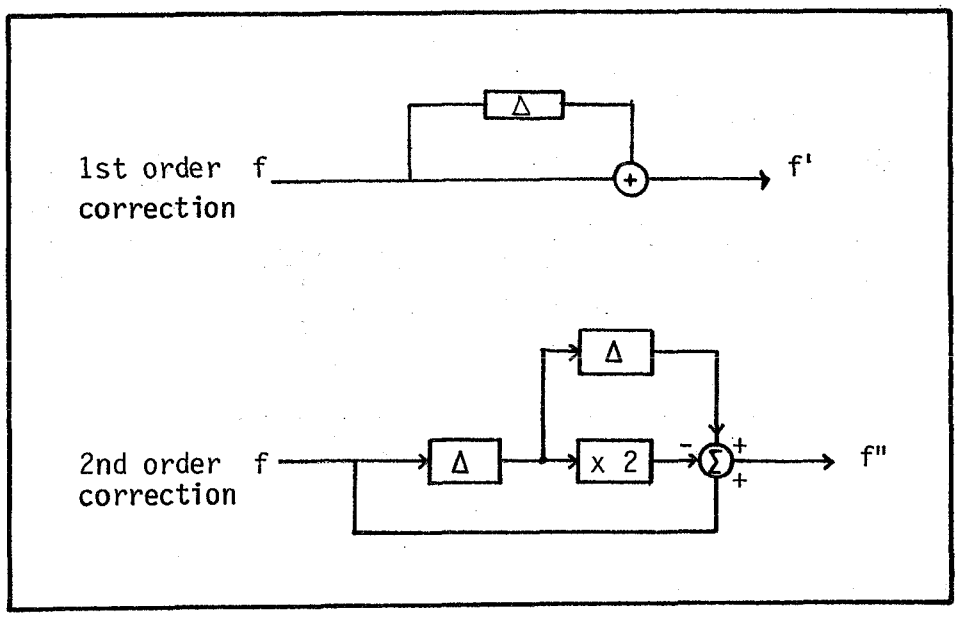


Fig. 7-2. Circuits for producing f' and f"

2nd order horizontal correction is very often implemented using only one delay line :

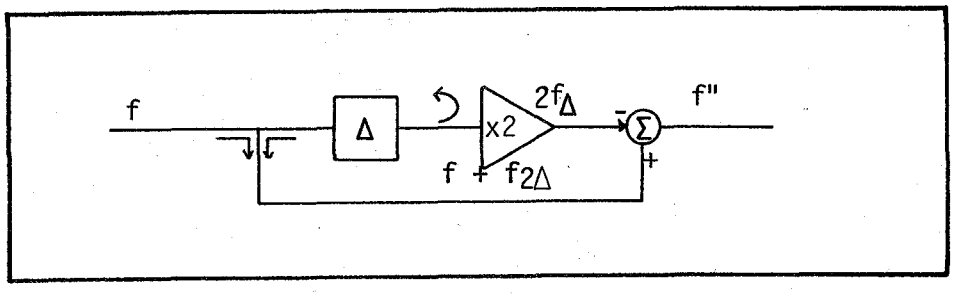


Fig. 7-3. Simplified circuit for making f"

Since the delay line is not terminated but open, the signal is totally reflected and delayed another time.

An aperture corrector is normally followed by a threshold circuit, which does not pass low-amplitude signals. Since aperture correction emphasises the high frequencies, noise increases also. Most of the noise and only little of the correction signal fall below the threshold.

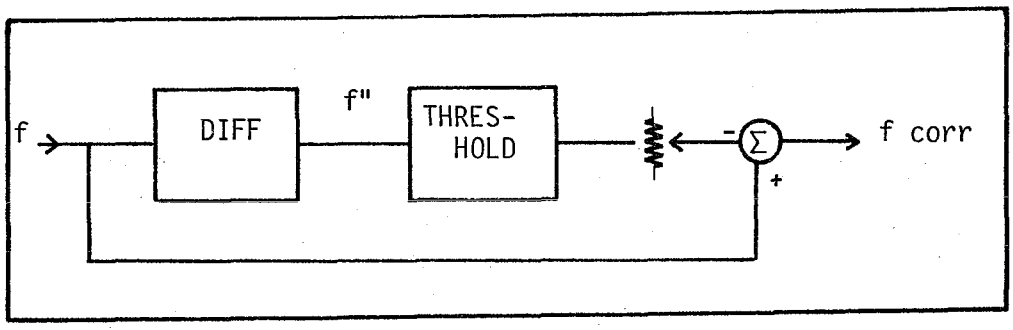


Fig. 7-4. Complete aperture correction circuit

7-2. Horizontal aperture correction

In the DXC-1800P it is of the 2nd order type with one delay line of 180nsec. All active circuitry is inside IC2, CX815.

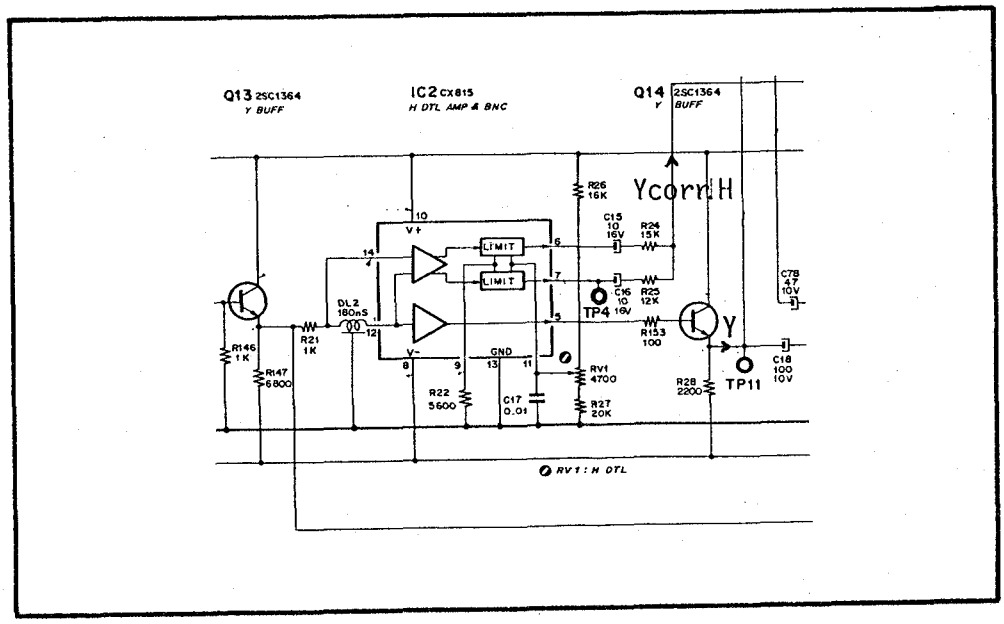


Fig. 7-5. Horizontal aperture correction.

The noise-canceller circuit is separate for the positive and negative portions of the signal. The threshold level is adjusted with RV1.

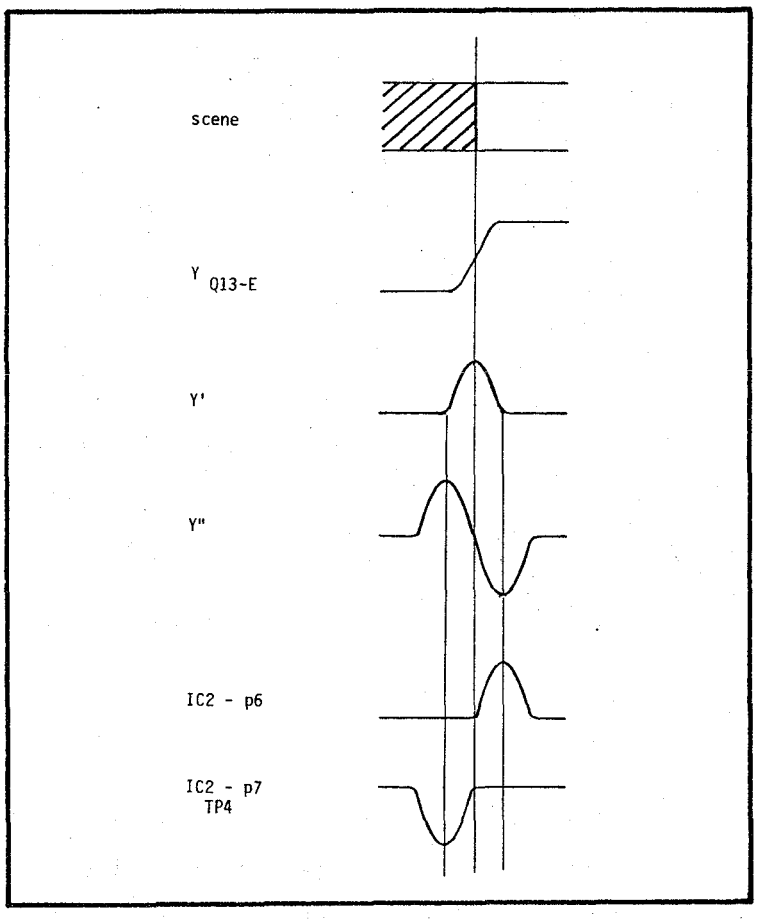


Fig. 7-6. IC2 output signals.

The two signals come out at pin 6 and 7 and are again mixed.

7-3. Vertical aperture correction

is only of the first order in the DXC-180OP but it is already an improvement over previous DXC cameras. A 1H delay line is necessary and two frequency convertors, because the baseband Y signal cannot be fed directly to a glass delay line.

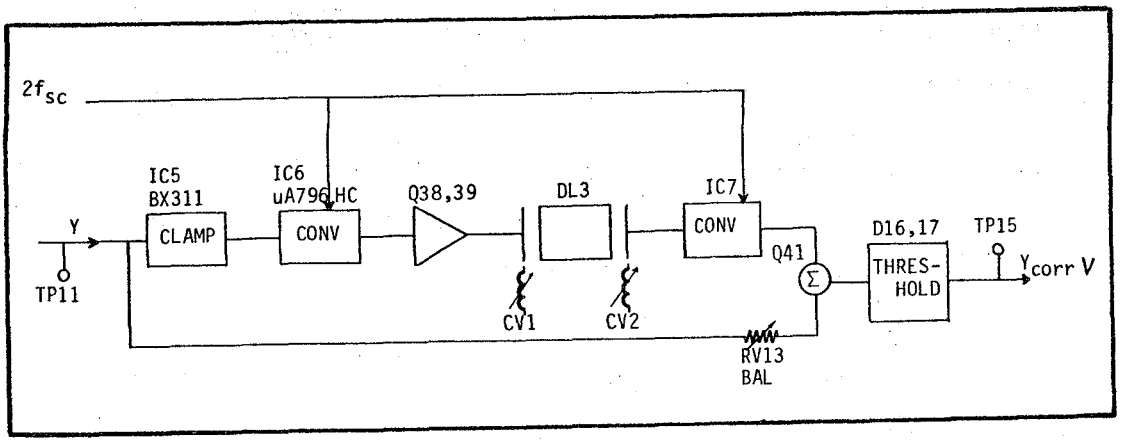


Fig. 7-7.

The "local oscillator" signal for the frequency conversion is simply 2fsc from the sync generator. LV1, 2 and RV13 balance the direct and delayed signals. The amount of vertical correction is determined by R130.

Line crawl compensation

Line crawl is a difference in DC level on alternate lines, and is caused by unbalance in the trinicon tube indexing circuit. It can be eliminated by subtracting the (Y_{direct} - $Y_{1H\ delay}$) difference signal from Y after passing it through a limiter.

7-4. ABL (Automatic Black Level)

The DXC-1800P is the first institutional camera from SONY to be equipped with an ABL system. The purpose is to improve the contrast for scenes with a limited dynamic range.

The principle is to limit the maximum level of the darkest picture element.

Normally (ABL OFF), black level is set by clamping black mask level (dark current) to the required pedestal level.

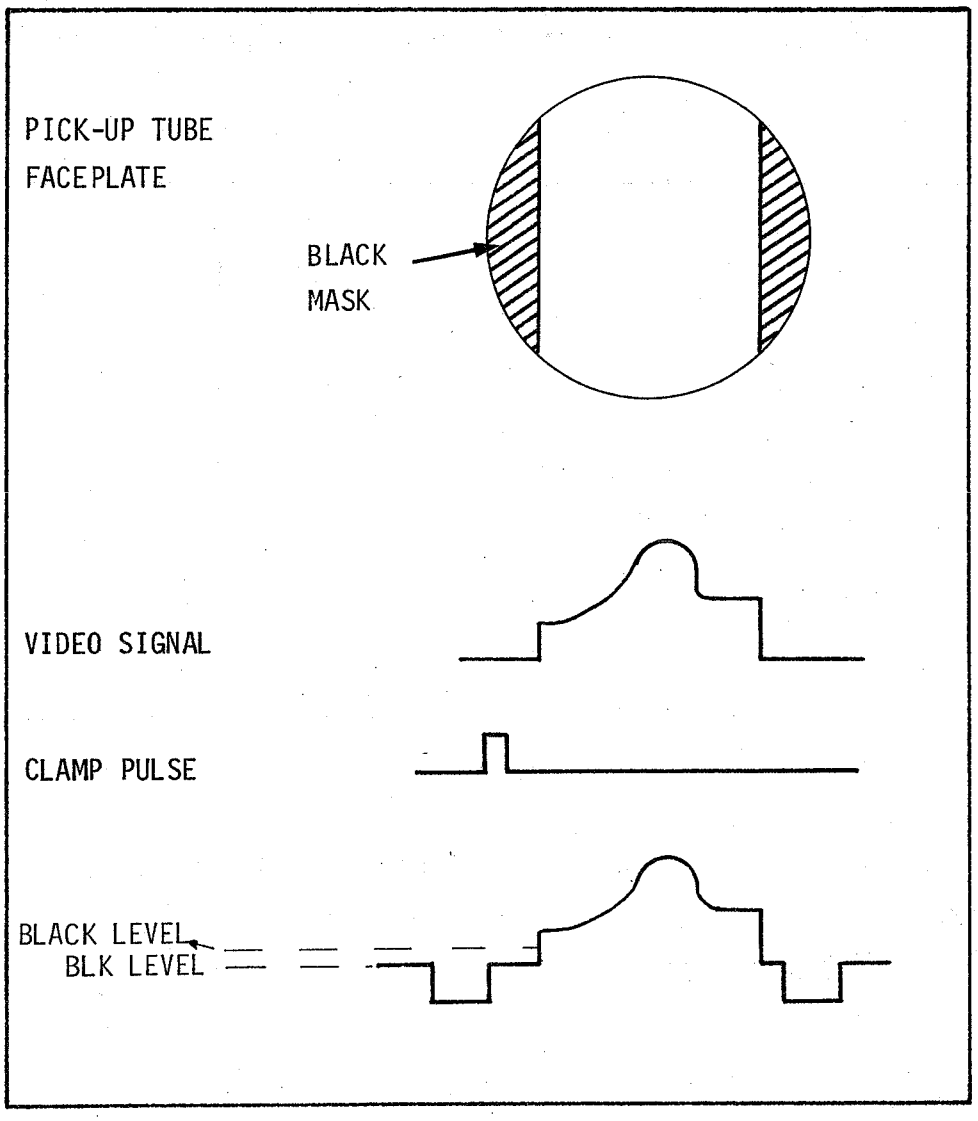


Fig. 7-8. Pedestal setting by clamping the black mask portion.

When shooting a scene with no dark portions, poor contrast results.

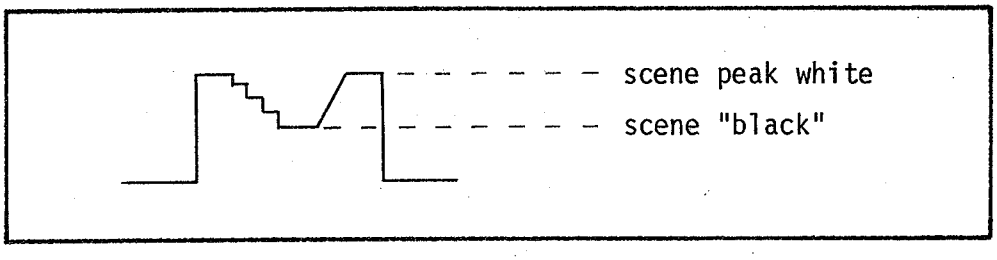


Fig. 7-9. Video signal when shooting scene with limited dynamic range.

When the ABL is switched on, this circuit lowers the black clamp level of the video signal before it enters the gamma correction circuit.

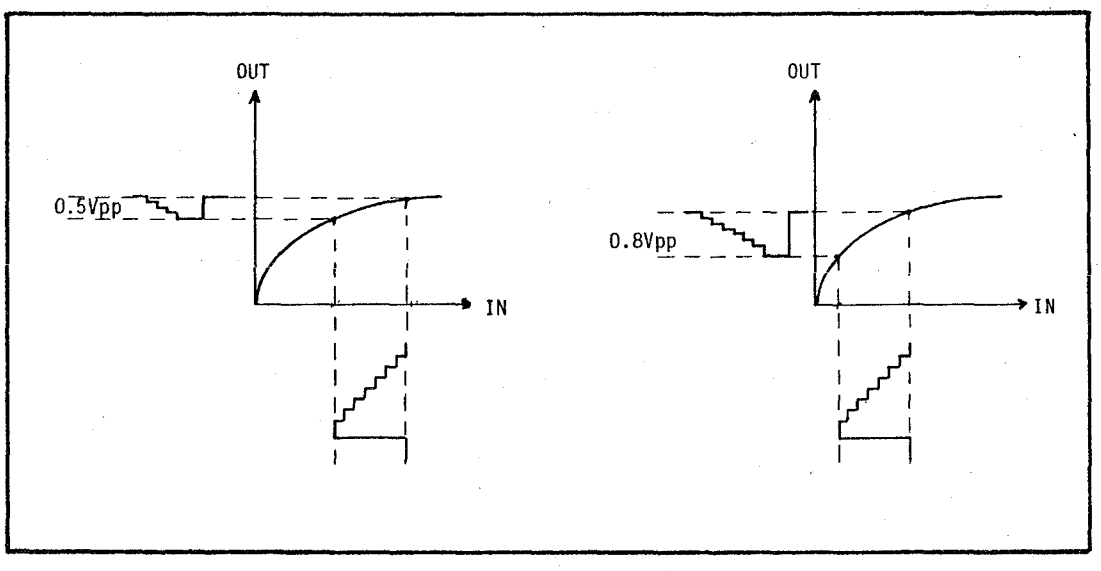


Fig. 7-10. ABL and gamma-correction.

The video signal is expanded and the peak level only slightly reduced. ABL acts on the active picture area and not on the black mask portion.

8. C PROCESSING

8-1. Functions

- pre-process
  - chroma suppress
  - band-pass-filter
  - chroma gamma

- standard trinicon decoder
  - comb. filter (Chroma - index separation)
  - index correction
  - chroma cancel
  - index alternator
  - 4.5MHz BLK osc.
  - synchr. demod.

- W/B correction

- CB generator

- PAL encoder
  chroma limit (knee)

The chroma is first separated from the output signal of the Trinicon tube by means of a 4.5 MHz band-pass-filter. It is then demodulated to give R-Y and B-Y colour differences. These are then encoded on the PAL subcarrier. Beside these standard functions we find following blocks in the DXC-1800P.

8-2. Chroma suppress

This means that the chroma signal is reduced by means of a LPF on the trinicon signal in case of low-light in +12dB or auto-mode. Otherwise the noise would drown the signal. However, it is not implemented in the first serial numbers.

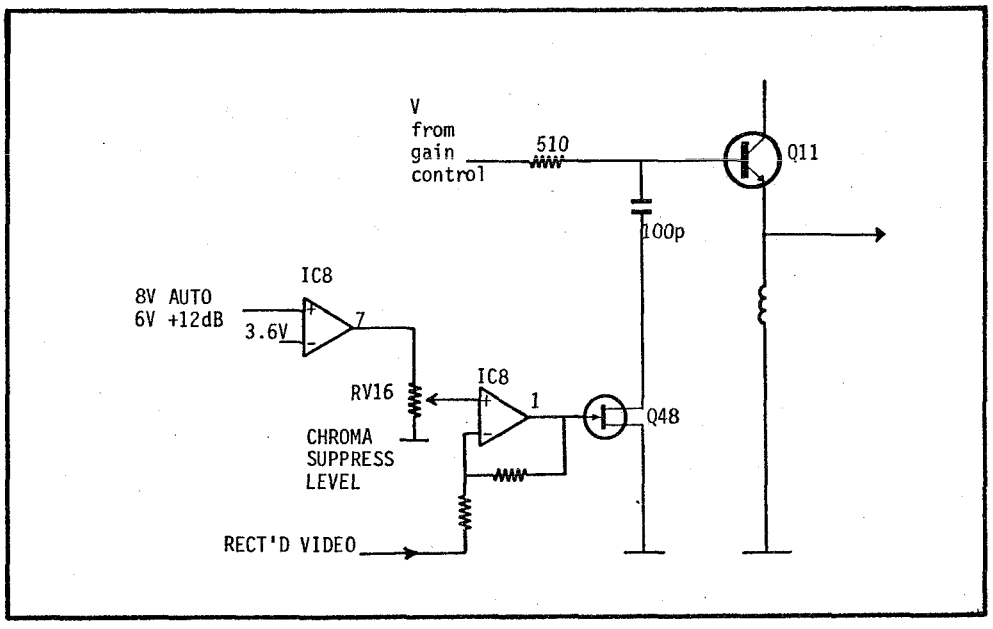


Fig. 8-1. Chroma suppress.

8-3. Chroma "limiting" (knee)

This circuit can be compared to white clip in the luminance channel. It reduces the chroma gain dynamically if Y exceeds a certain level. This is done inside the encoder IC10, CX873.

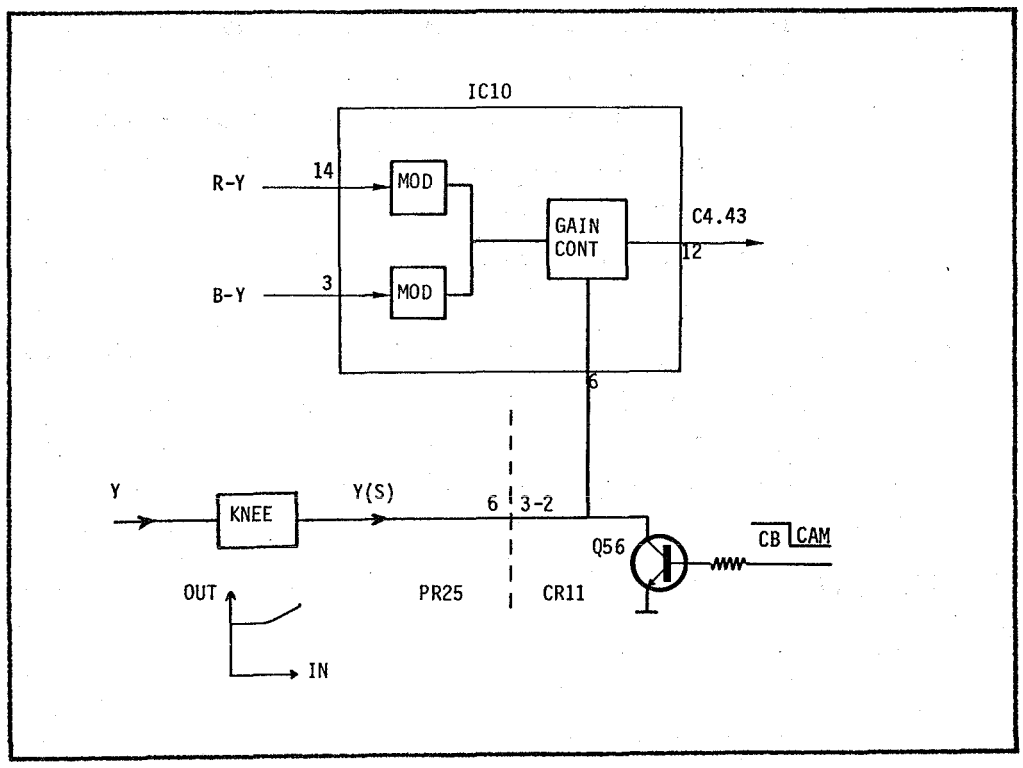


Fig. 8-2. Knee (Chroma limiting).

Y is passed through a knee or "soft threshold" circuit. If Y(S) increases, C goes down.

8-4. Colour-bar generator

The DXC-1800P can be put into colour-bar mode locally, or remotely from the control unit. (Local switch is disabled.)

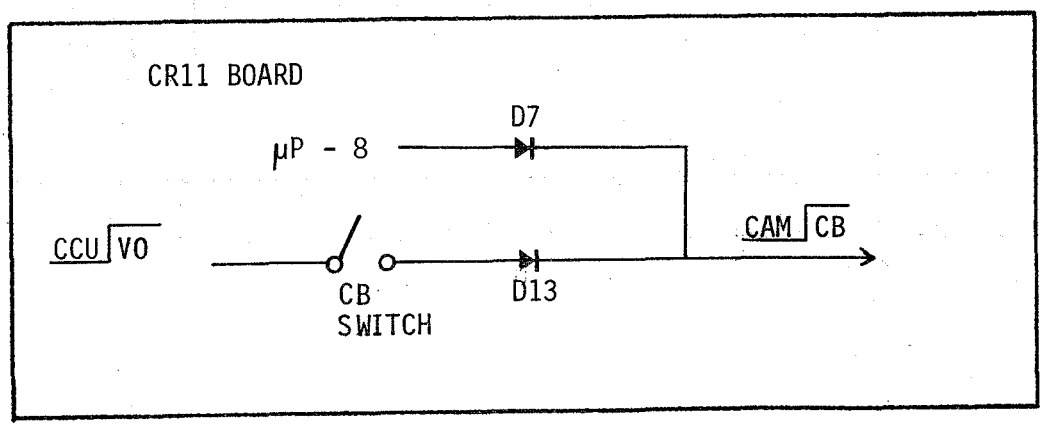


Fig. 8-3. Colour bar ON/OFF circuit.

Following actions take place :

- the iris is closed (if not under manual control)
- the colour-bar generator is enabled
- Y, R-Y, B-Y signals going to the encoder are switched using an analog switch IC9, TC4053. (Switch is random and not in vert. blk.)
- The chroma gain-modulator is muted.

The CB generator is adjusted for 100/10/75 colour bars, which means

- 100% white bar
- 10% pedestal
- 75% R, G, B before matrixing.

Following figures show the principles :

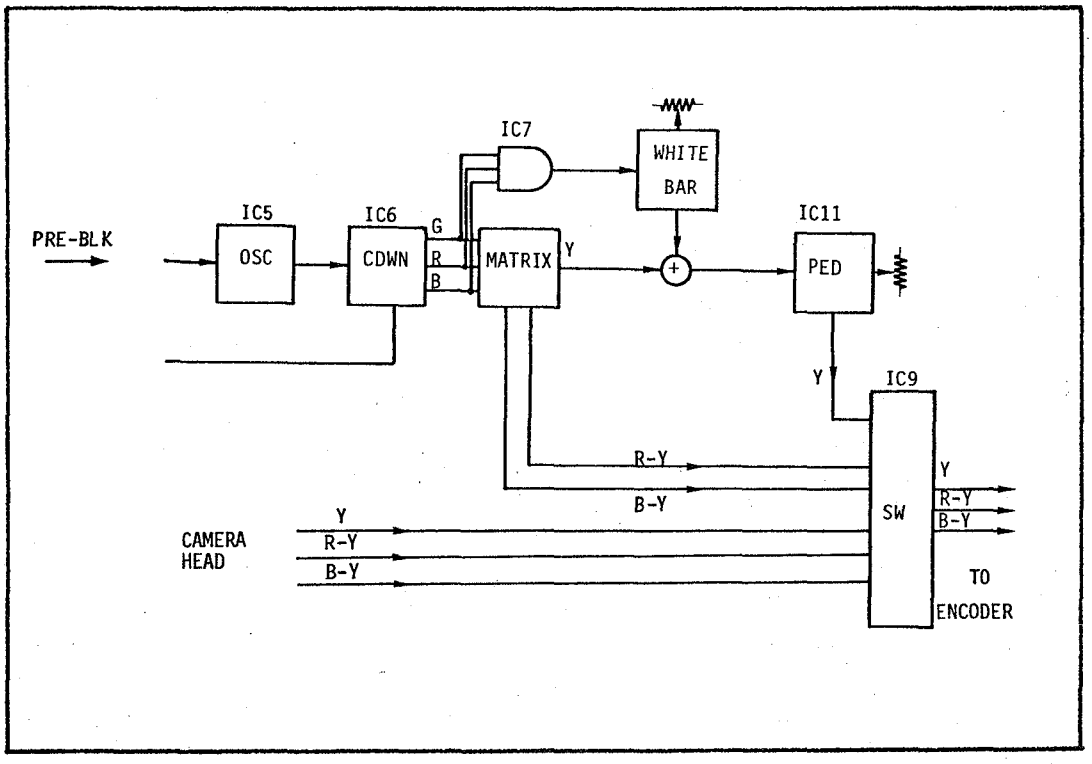


Fig. 8-4. Colour bar generator block diagrams

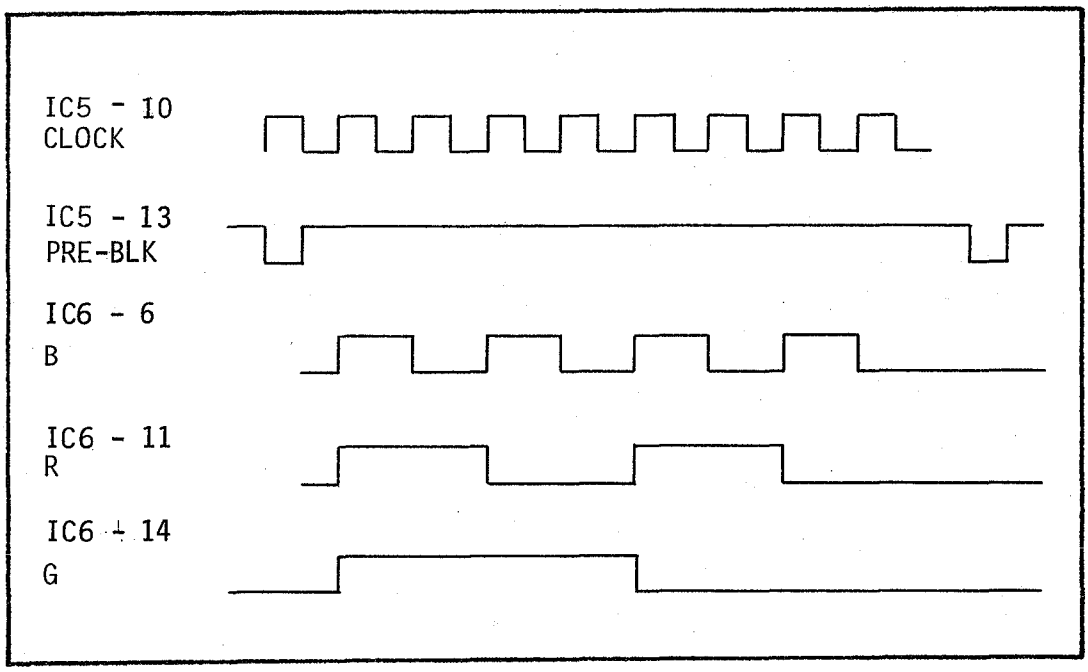


Fig. 8-5. Colour bar generator waveforms.

The oscillator is made from C-MOS NAND gates and has a frequency of about 9.5 f_H. The counter is enabled when both the PRE-BLK signal at IC5-13 and CB-ON signal at IC5-12 are high. The outputs are R, G, B. These are matrixed into Y = 0.3R + 0.59G + 0.11B and R-Y, B-Y. The white-bar is detected and its level can be adjusted independently. After clamping and pedestal off-set on Y, the signals proceed to the encoder.

9. MICROPROCESSOR FUNCTIONS

9-1. The Microprocessor :

The processor used is a 4 bit all-in-one-chip CMOS from Hitachi : the HMC 43C. The chip used in the DXC-1800P is labelled HD44750A28.

Following are the specifications :
42 pin DIL
power supply/consumption :
operation mode : 5V ± 10% / 1mA (5mW)
standby mode : 2V / 1.0µA
In standby mode the static RAM memory is preserved.

on chip memory :
ROM program : 1024 x 10 bit
pattern : 64 x 10 bit
RAM : 80 x 4 bit

clock frequency Fcp = 400
execution speed : 10µsec.

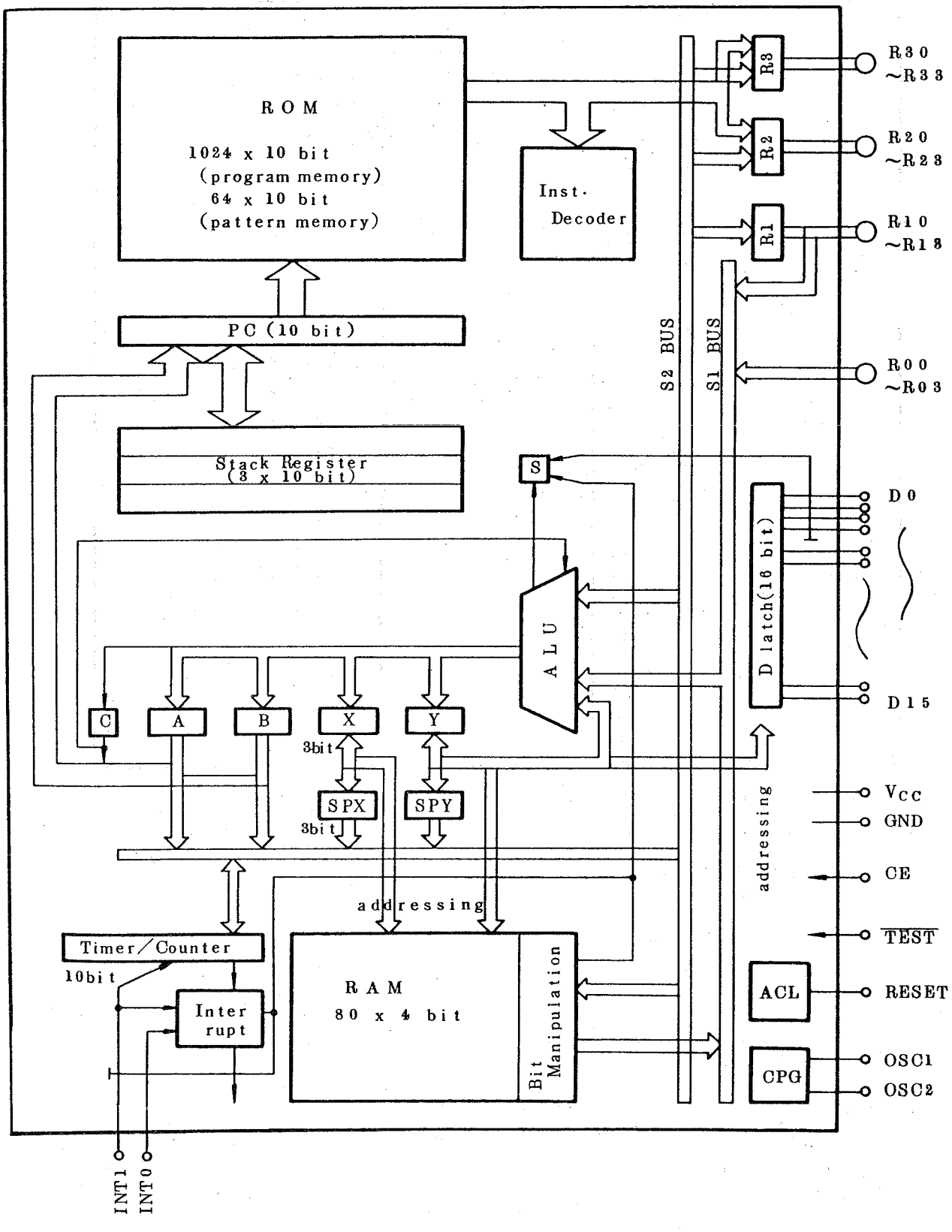


Fig. 9-1. HMCS43C Architecture.

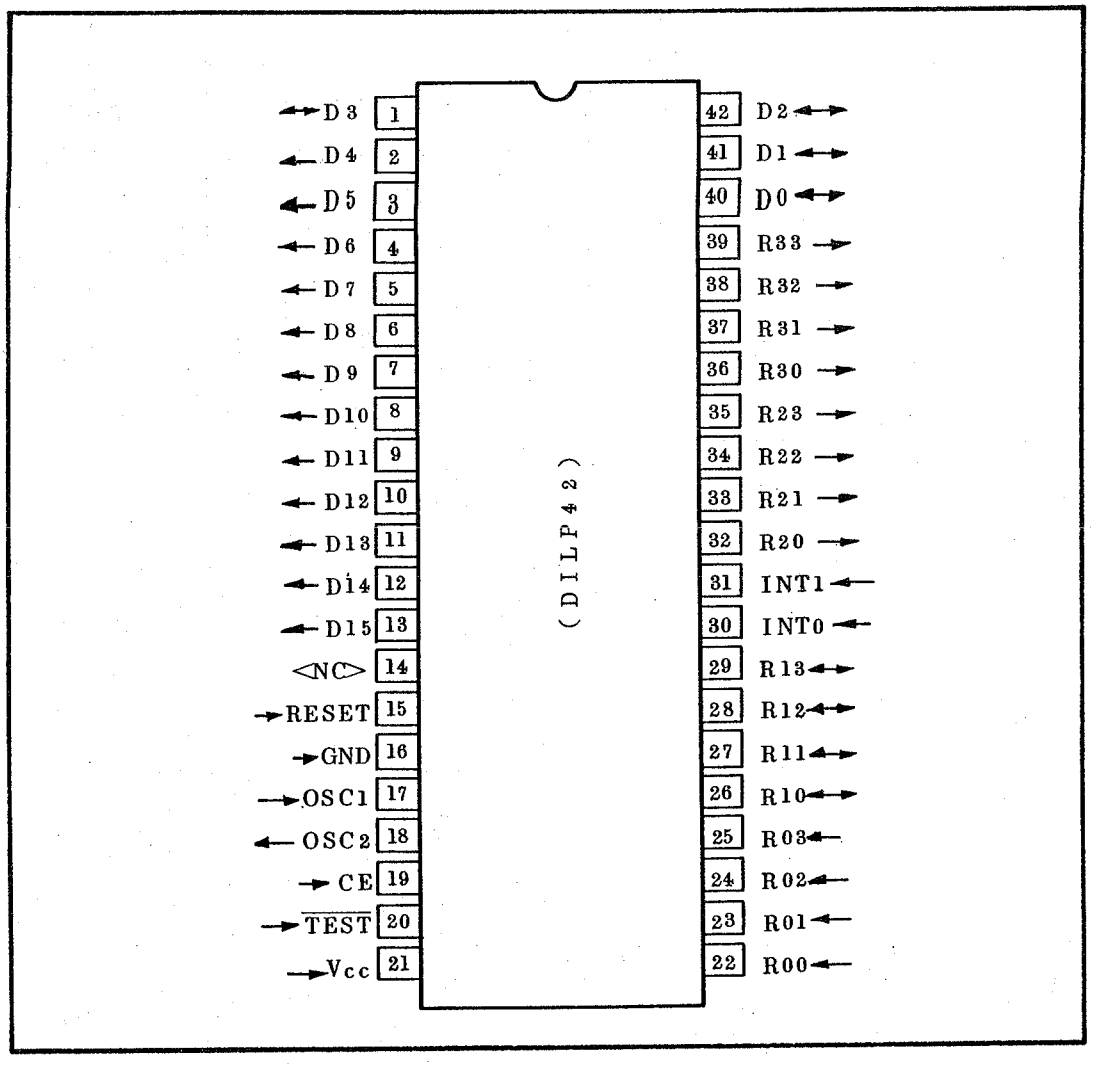


Fig. 9-2. HMCS43C Connections.

9-2. Auxiliary circuitry

-power p 16 ground

p 21 + 5 or + 2V

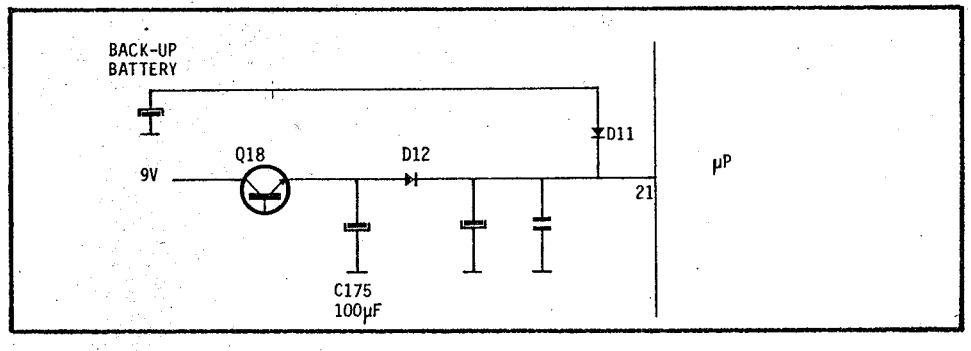


Fig. 9-3. Power supply to the microprocessor.

Normally 9V is dropped to 5.5V in Q18. (D12 is necessary and so the 5Volt supply rail cannot be used.) In standby mode power comes from the back-up battery : MERCURY, 2,7V, type 2MR44. Capacity is sufficient for about 2 years. Without the battery, there is already 5 min. back-up from C175.

$$\frac{dV}{dt} = \frac{I}{C} = \frac{10^{-6}}{100\ 10^{-6}} = 0{,}01\ V/sec.$$

3Volts corresponds to 300sec = 5 min.

- clock oscillator : a 400 KHz crystal is connected between p 17 and p 18.
- Test input p 20 is not used and connected to 5V.
- RESET p 15 is made high at power on, to start the processor in the monitor program.
- CHIP ENABLE p 19 is normally high (operation mode). When low, the chip is in standby mode and voltage at p 21 may be reduced to 2V.

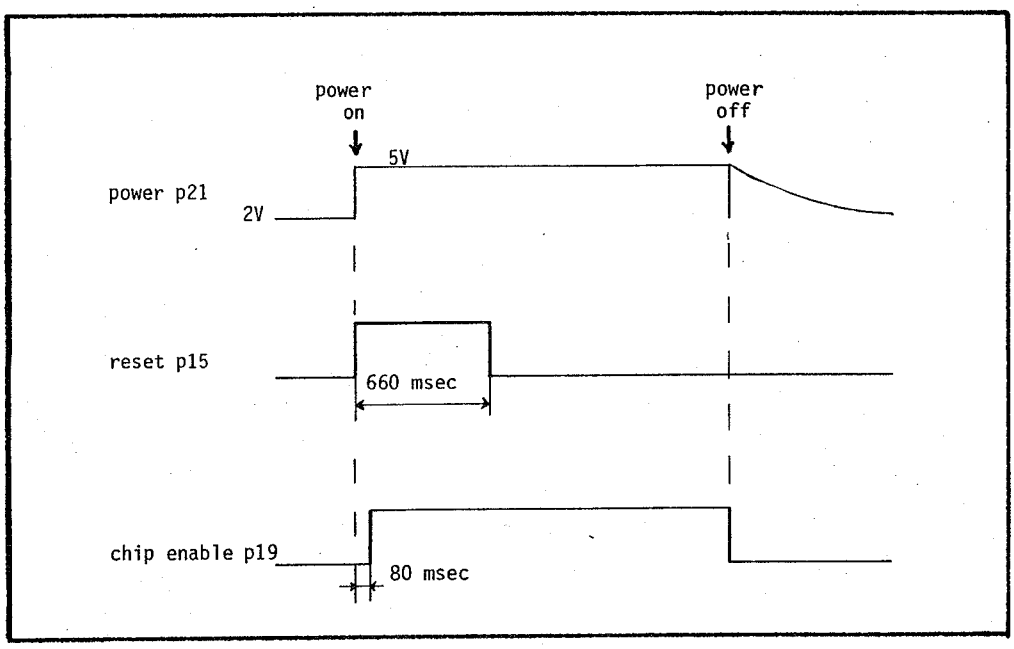


Fig. 9-4. Timing of reset and chip enable.

When the microprocessor is suspected, it is advisable to check all these inputs.

9-3. Phases

The same microprocessor is used in the control unit CCU 1800P and in the camera head DXC-1800P. Also, the microprocessor in the camera has different functions according to whether a video-recorder or the control unit is connected. This means that the microprocessor contains three different programs. Actually some subroutines are in common so it is better to say there are three monitor programs or phases.

CCU phase : p1 and 29 grounded
CHU phase : p1 and 29 open.

The distinction between DXC-VO and DXC-CCU phase is made by the absence/presence of a serial data burst on pin 10 of the CCQ connector.

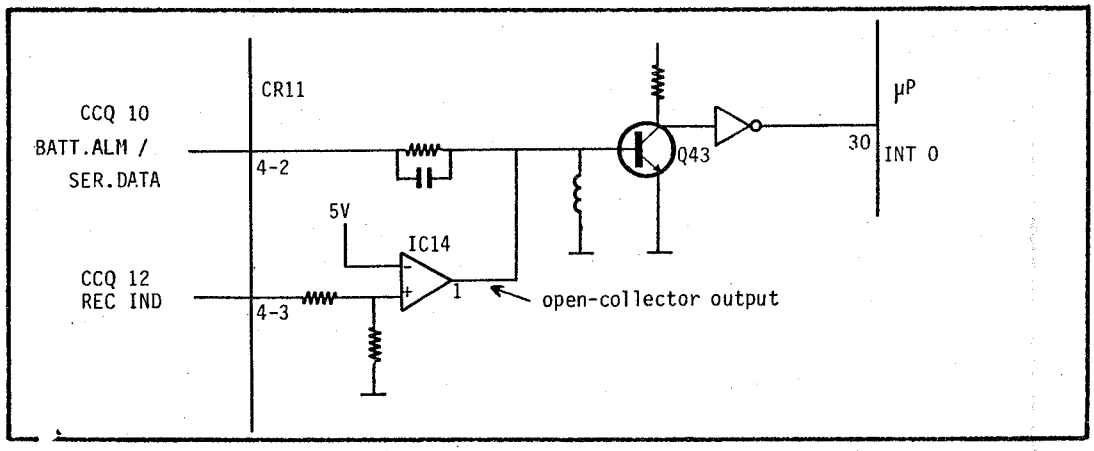


Fig. 9-5. Microprocessor / CCQ cable interface.

With a VO-4800P connected, the CCQ12 line carries the REC IND signal which is 0, 2,5 or 5V. Then IC14-1 is L (0V), and μP-30 is L. Also with the CCQ cable disconnected, μP-30 is L and the DXC-VO phase results.

When the control unit is connected, CCQ12 is at 12V, IC14-1 is open and CCQ10 serial data input is passed to μP-30. At the first burst of serial data the microprocessor goes into DXC-CCU mode.

9-4. Common Functions

The microprocessor performs following functions :

DXC-VO mode	W/B-memory
	-automatic adjustment
	fader
CCU mode	A/D convertor
	transmitter
DXC-CCU mode	receiver
	D/A convertor
	auto-W/B

Actually both camera and control unit contain a complete A/D - D/A convertor :

The D/A convertor consists of a ladder network. The analog output may vary from 0 to 5V in steps of $\frac{5V}{156} \approx 20mV$.

00 hex corresponds to 0V
80 hex corresponds to 2.5V
FF hex corresponds to 5V (-20mV)

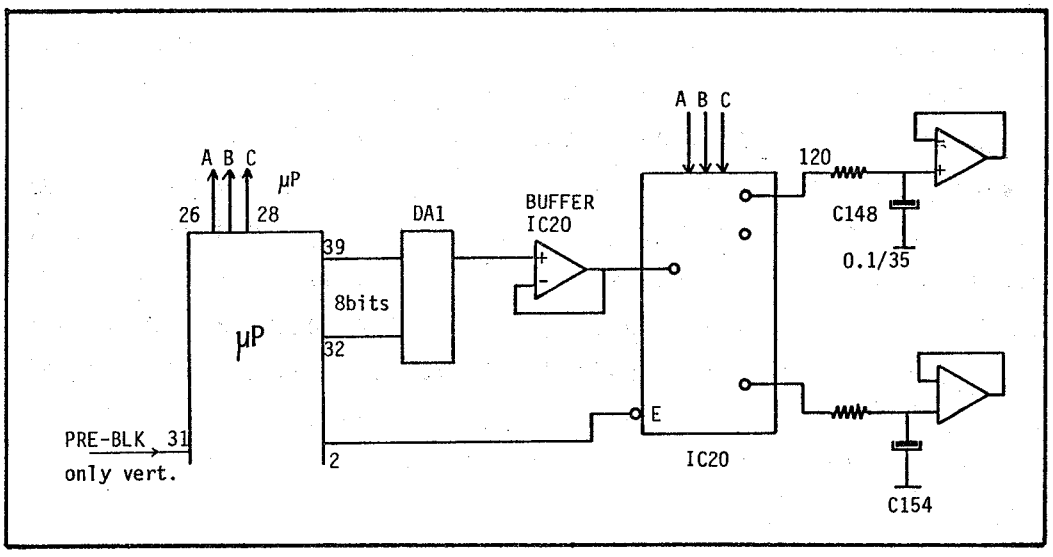


Fig. 9-6. D/A Conversion and refresh

There are 8 analog outputs. The binary codes are multiplexed on the µP data outputs. After D/A conversion, analog switch IC20 (TC4051BP) demultiplexes the analog signals which are stored on hold capacitors C148 - C154.

A B C	Decimal	TC4051 channel pin	analog input	analog output
0 0 0	0	S_0 13	R-Y	± YR
1 0 0	1	S_1 14	B-Y	± YB
0 1 0	2	S_2 15	BLK	C level
1 1 0	3	S_3 12	FADE time/off	FADE level
0 0 1	4	S_4 1	/	PEDESTAL
1 0 1	5	S_5 5	/	HOR. PHASE
0 1 1	6	S_6 2	/	SC. PHASE
1 1 1	7	S_7 4	/	IRIS

Beside the ABC selection lines, the TC4051 IC has an ENABLE input. The analog connection is only made when this input is high. This is controlled by the microprocessor and occurs in the vertical blanking period. This means there is a certain cycle so that the condensors storing the analog signals are refreshed during V.BLK, different signals on successive fields. The buffer IC's are BIMOS with JFET input so that the voltage does not change appreciably. The timing reference is provided by a vertical pulse at pin 31 of the µP, which is an interrupt. This pulse is derived from PRE-BLK by removing the horizontal pulses.

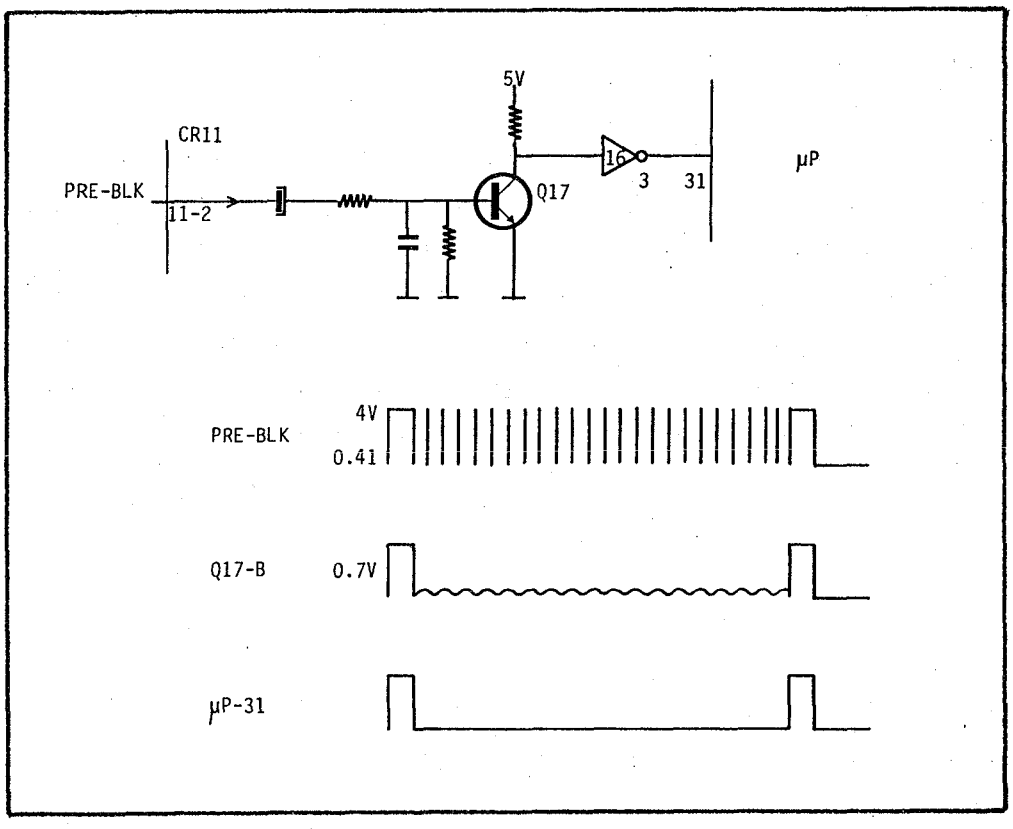


Fig. 9-7. Timing reference for the processor.

On the A/D side, we find a multiplexer (also TC4051) and a comparator IC17, C17, μP311C. The conversion is done by successive approximation (bit-by-bit) under microprocessor control, using the D/A convertor.

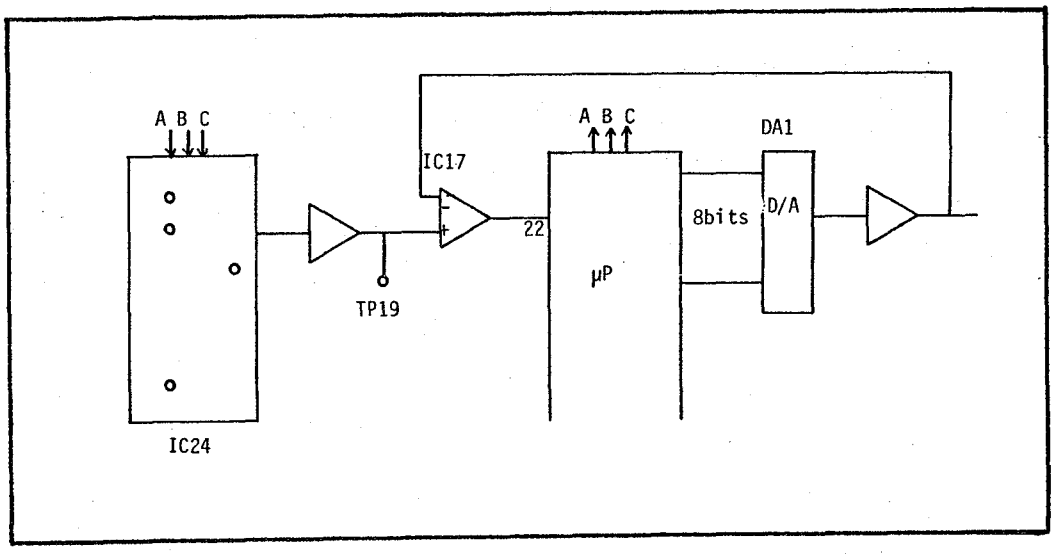


Fig. 9-8. A/D Conversion.

Memories :

In VO mode the last five control signals are not used, they are disconnected from the circuit. Chroma level is at a preset value of 80.

The ΔY control signals depend on the W/B switch. In preset they are at 80 hex or 2.5V. Otherwise, the internal memory is used. At power on, the microprocessor performs certain checks to find out whether back-up is still effective and the data stored in memory valid. If yes, then this data is used for W/B control. If not, then the memory is set to preset 80 hex. At each pressing of the AUTO W/B switch the microprocessor goes through a series of operations to determine the new white-balance values, and puts these in memory.

9-5. Auto-white-balance

The principle of white-balancing is the same as for previous cameras :

A suitably attenuated Y signal ΔY is added to or subtracted from R-Y/B-Y. Only now, all steps are carried out by a microprocessor instead of the cameraman. It consists basically of measuring the chroma signal during peak white and adjusting $\pm \Delta Y_R$ and $\pm \Delta Y_B$ until chroma is zero at that point.

Beside the microprocessor, an A/D - D/A interface is needed so that analog signals can be handled (analog inputs : R-Y/B-Y, analog outputs : $\pm \Delta Y_R$, $\pm \Delta Y_B$), and a peak white detect circuit that tells to the processor when a peak-white portion of the scene is being scanned.

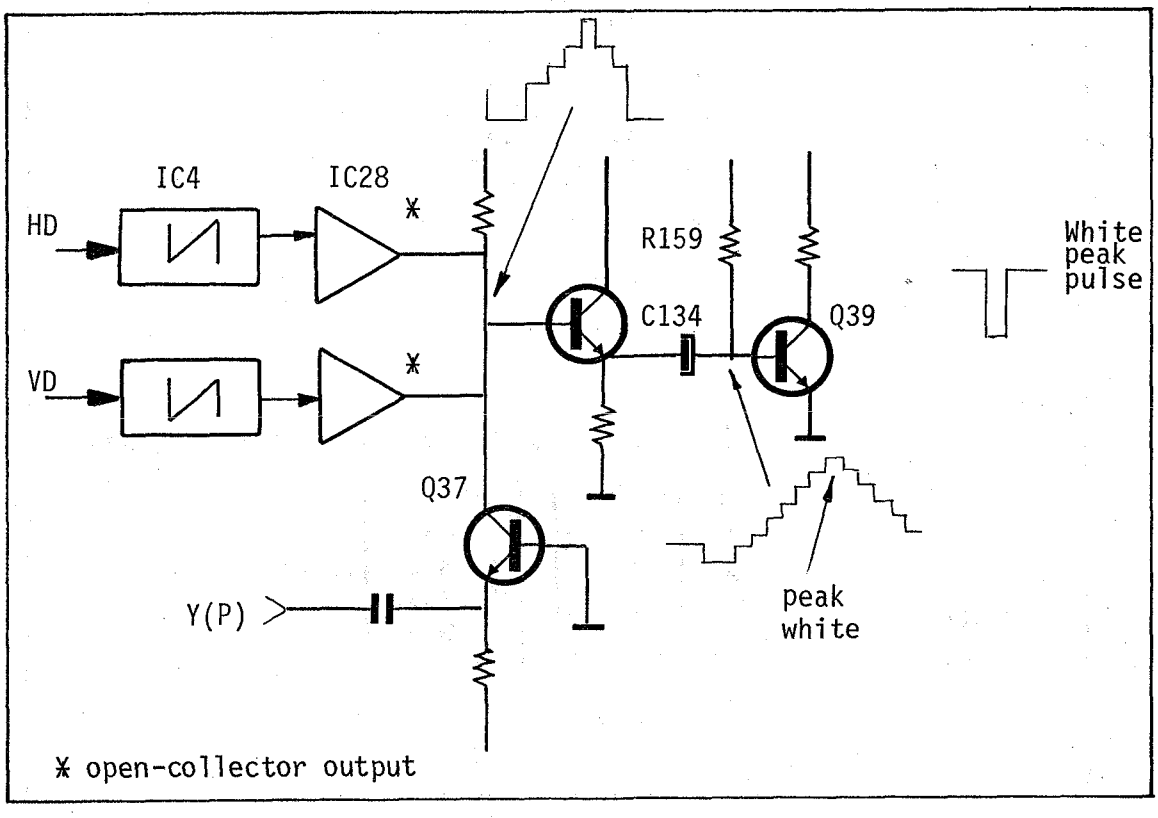


Fig. 9-9. Peak white detector.

The circuit of C134, R159, Q39 looks like a sync separator, but because of the opposite polarity of the video signal it is the peak white that produces an output pulse.

The circuit is enabled by a window gate pulse that restricts the white-balance operation to the center of the picture.

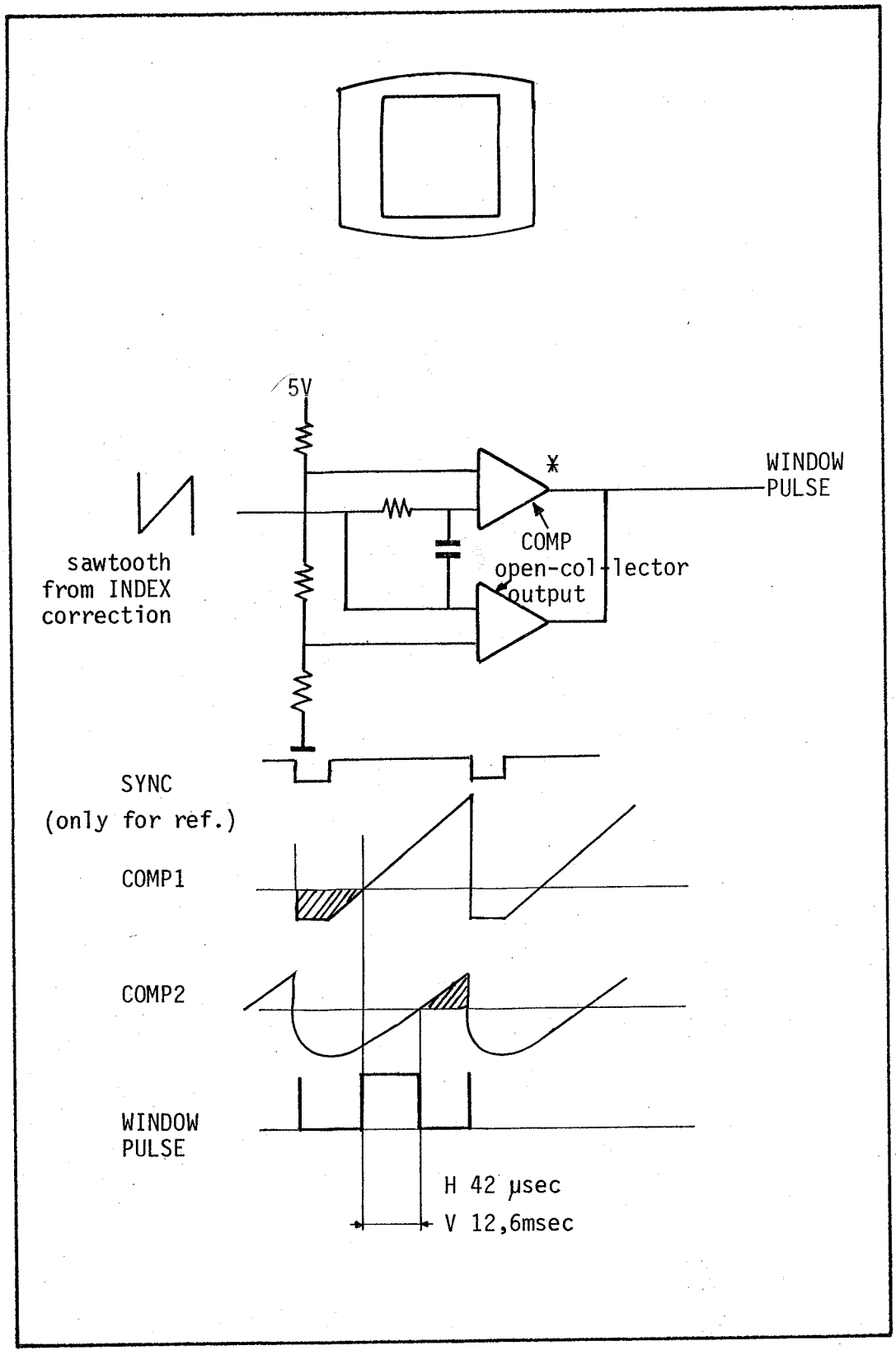


Fig. 9-10. W/B Window circuit

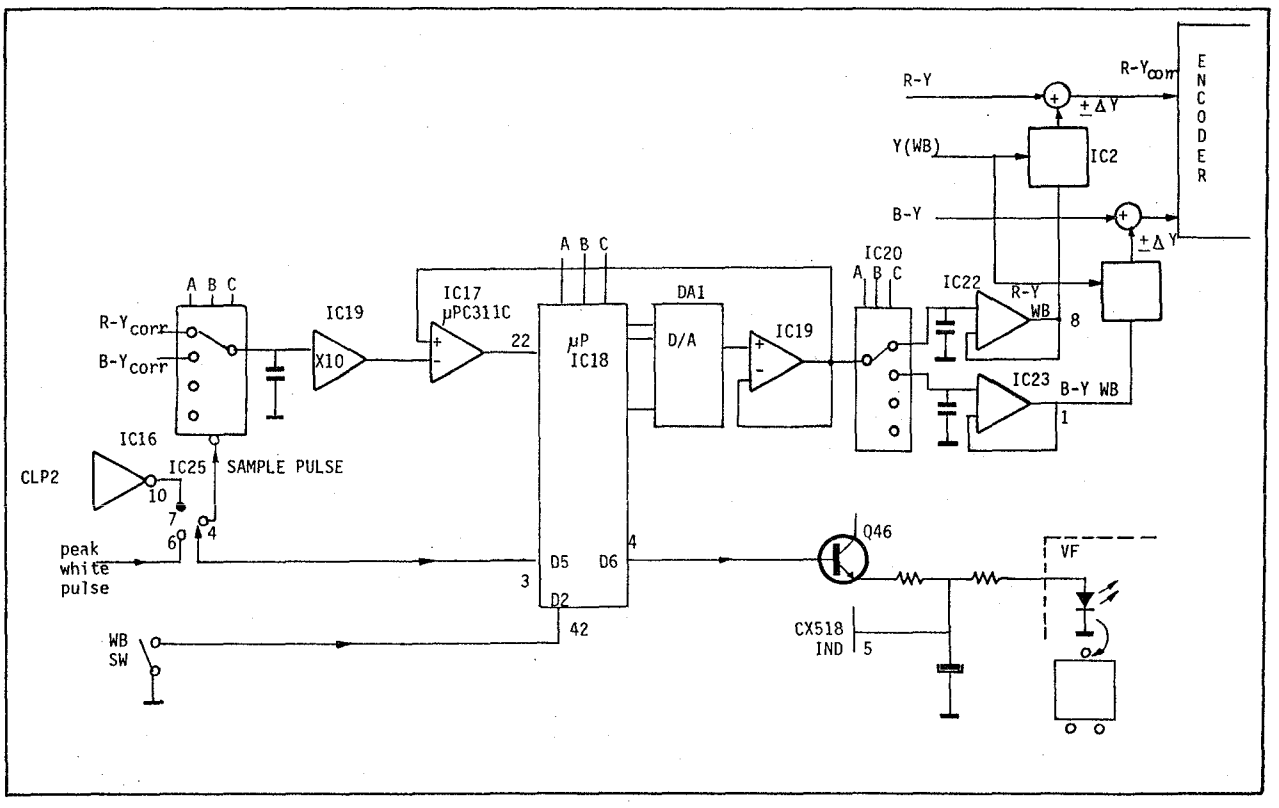
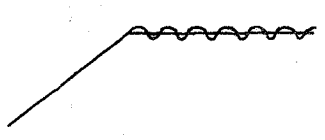


Fig. 9-11. Auto-white-balance block diagram.

When the auto-W/B switch is pressed, the following sequence starts (it is not necessary to hold the switch).

-Set ΔY_R to preset value "80" (RV5/6 are adjusted for correct W/B at 3200°K, filter 1).
-sample R-Y (CLP2) → A/D → store → V_C
-sample R-Y (white pulse) → A/D → store → V_W
-change Y_{R-Y} W/B A → D until $V_W = V_C$
-



LSB changes 0 → 1
15 times then OK

-Same operations for B-Y
-light W/B indication

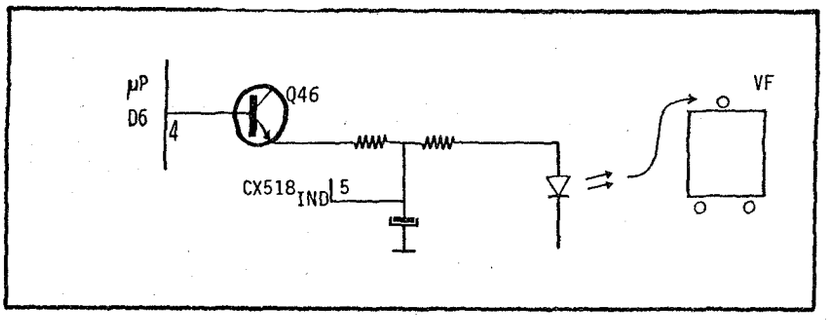


Fig. 9-12. W/B indication.

On the vectorscope the following trace is observed.

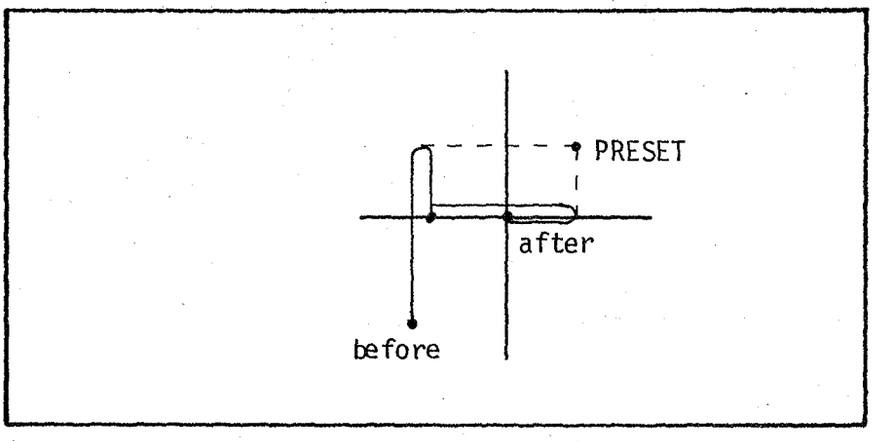


Fig. 9-13. W/B on vectorscope.

The procedure is self-adjusting for carrier offset since the colour difference signals are sampled in the blanking period, before the value during peak white is measured. The whole lasts about 7 seconds as shown in following figure.

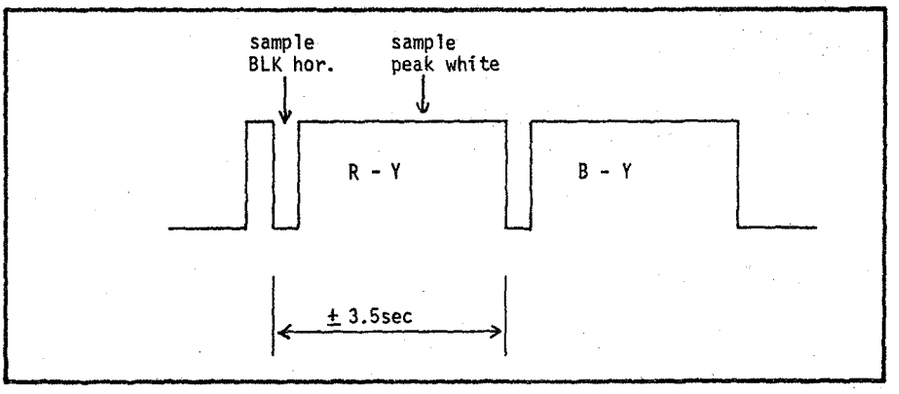


Fig. 9-14. R-Y/B-Y sample pulse select (μP-3 = IC25-2).

9-6. Fader

Fading means increasing the video level slowly up to normal level (fade - in). Only the Y and C signals are changed, burst and sync are mixed later at normal level. For a complete cycle, first output is decreased, then the VTR started and then the gain goes up slowly.

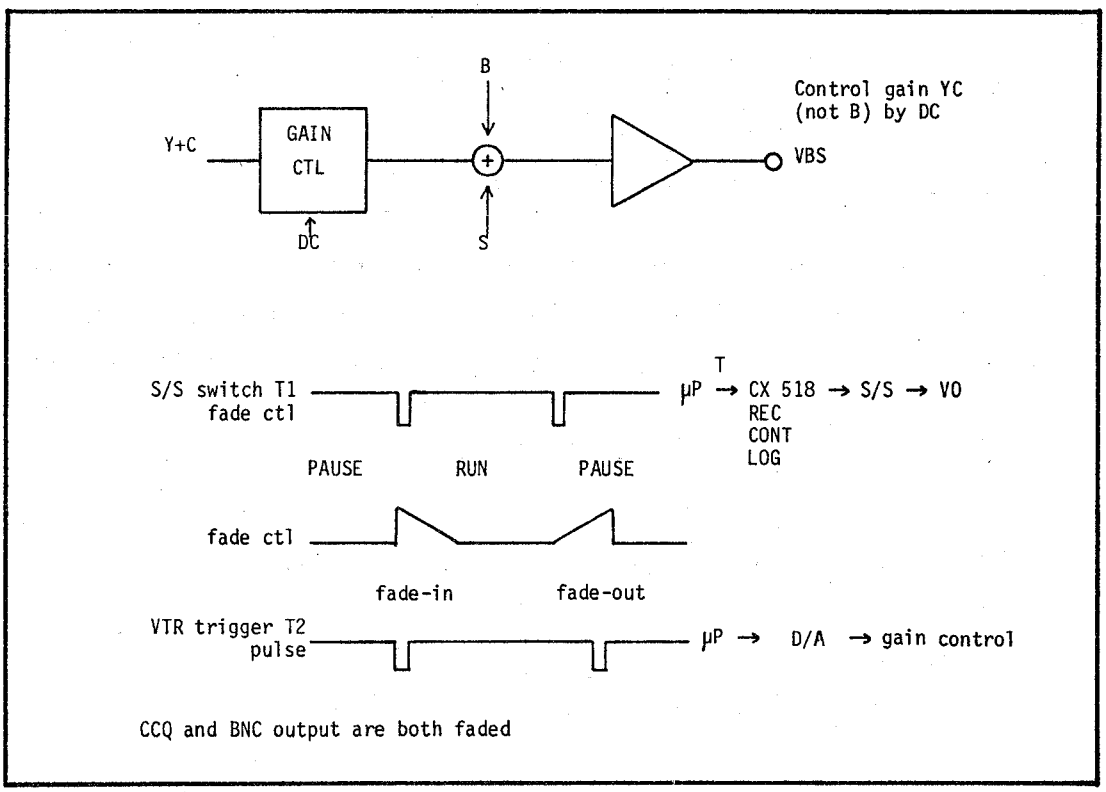


Fig. 9-15. Fader waveforms.

Fade control

The use of a microprocessor makes it possible to vary the fade time easily.

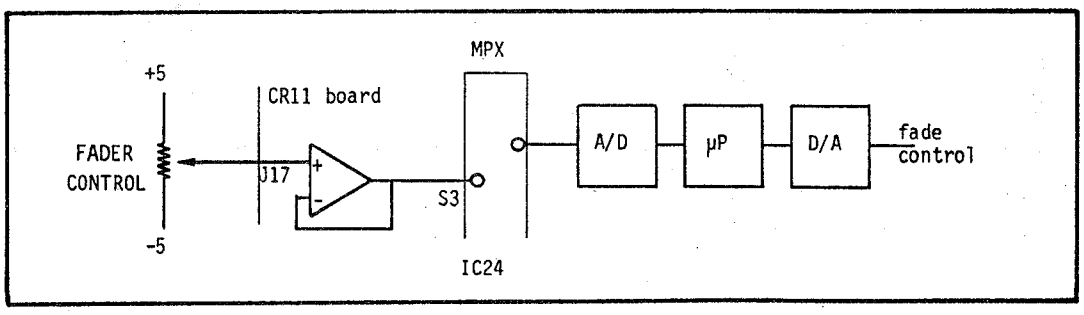


Fig. 9-16. Fade control.

The position of the fade control is converted into a binary value. Below a certain threshold there is no fading : the fade control also functions as fade on/off. The fade time is continuously variable from 0 to 5 sec. The microprocessor in turn produces a fade control output signal, which is related as follows to video gain :

digital	analog	gain
FF hex	5V	min
80 hex	2.5V	max
00 hex	0V	/

Like the other analog outputs it is obtained by D/A conversion and sampled in the V.BLK period. So it can only change by one step per field. If all 256 steps ($\sim$ 8 bits) are used, then the minimum fade time would be :

$$256 \times \frac{1}{50} \cong 5 \text{ sec.}$$

So for short fade times the control changes by several steps at a time, which corresponds to using less bits.
The shortest fade time is :

4 bits $\sim$ 16 steps $\times \frac{1}{50} \cong \frac{1}{3}$ sec.

Trigger timing

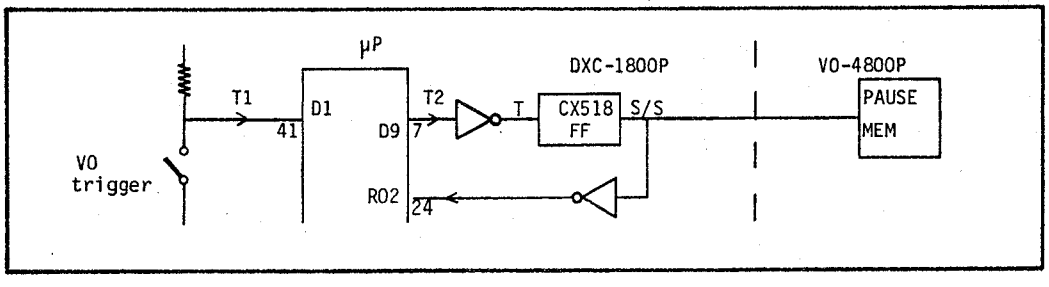


Fig. 9-17. Start/stop signals.

If PAUSE then
- gain min
- start
- fade-in

RUN then
- fade-out
- stop
- gain max.

In order to start fade-in or fade-out at the right moment, the trigger pulse passes through the microprocessor. Also the PAUSE | RUN returns to the µP.

Following flowchart shows the fader program in a simplified form.

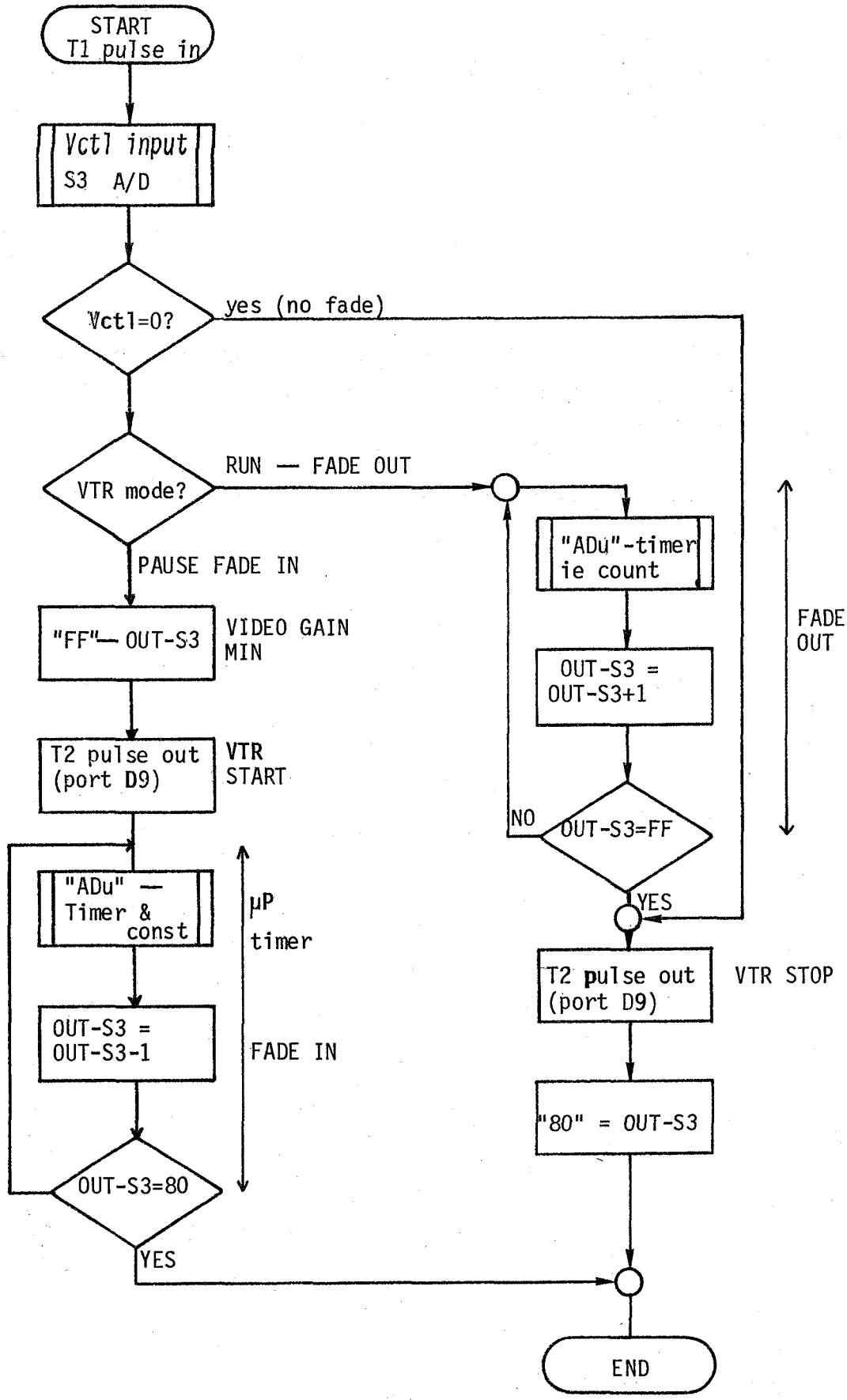


Fig. 9-18. FADE IN/OUT.

10. VTR INTERFACE

10-1. Signalling

In the CCJ system (VO-3800P - DXC-1600P) this consisted only of the start/stop (or run/pause) signal (CCJ-6).
Pause-memory is in the camera. The same connection serves for tally indication.

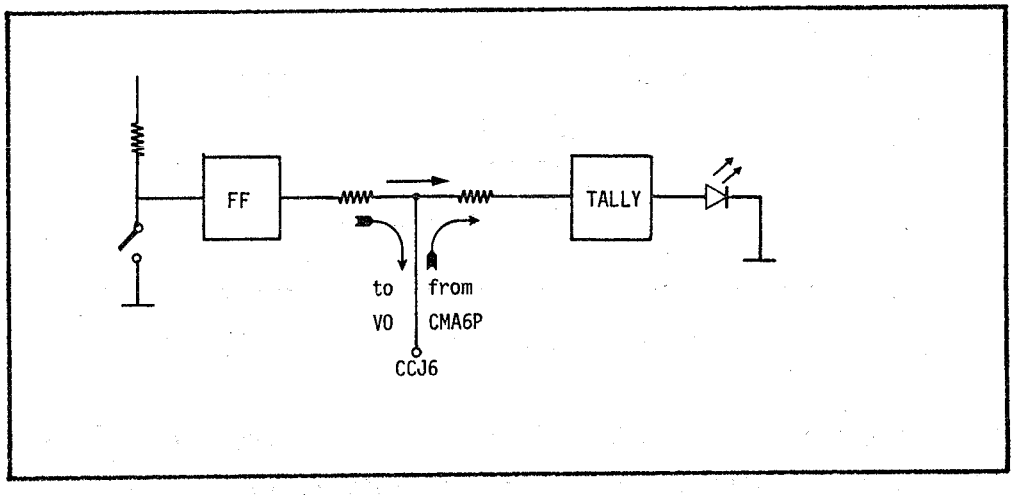


Fig. 10-1. Start/stop and tally in the CCJ system.

In the CCQ-system the actual run indicator returns to the camera separately. This line also carries the VTR alarm (servo, before-end).

CCQ13.	S/S	VTR ←
+ CCQ10	VO BATT IND	→ CAM
+ CCQ12	RUN IND/ ALARM	→ CAM
+ CCQ14	PB AUDIO f PB STATUS (DC)	→ CAM

In the DXC-1800P there is one additional feature : the camera own-battery low-voltage alarm (DC6).

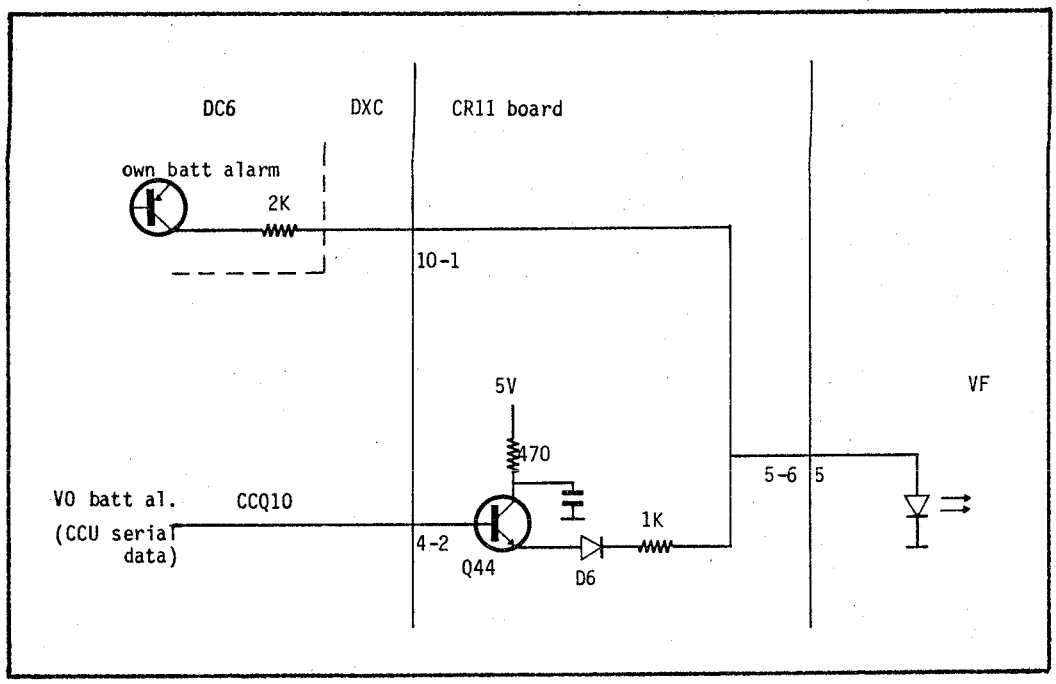


Fig. 10-2. DXC-1800P battery alarm.

The CX518 IC contains the RUN/PAUSE flip-flop and decodes the VO-indicator signal. (See appendix for more information.)

The three sets of waveforms apply to VO-CCQ, VO-CCJ and CCU modes.

10-2. Viewfinder

Universal mounting
8p connector
low-power consumption 2,3 W or 200 mA at 12V (switching regulator)

IC's	BX 311	video clamp and buffer
	CX 104	sync sep, Vert ox, beas AFC
	µPC 575	vert. amp.

HOT and HV integrated

Video	clamped
	peaking (ON/OFF)

Indicators

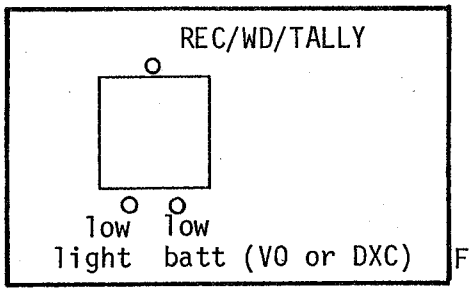


Fig. 10-3.

NB. Indicators in previous cameras are as follows :

1600/10 1 REC S/S, Tally

1650 2

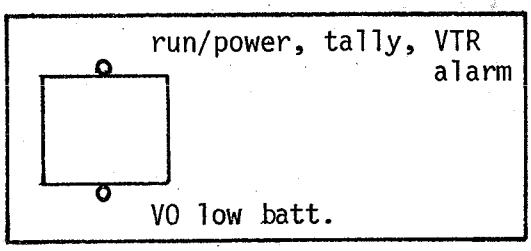


Fig. 10-4.

10-3. VF switch circuit

1600/1610

CCJ ↔
discrete
auto

1640

CCQ ⇄
discrete + CX518
switchable AUTO
VTR
CAM

1800

CCQ ⇄
discrete + CX518 + μP
switchable AUTO
VTR
CAM
return video by S/S sw.

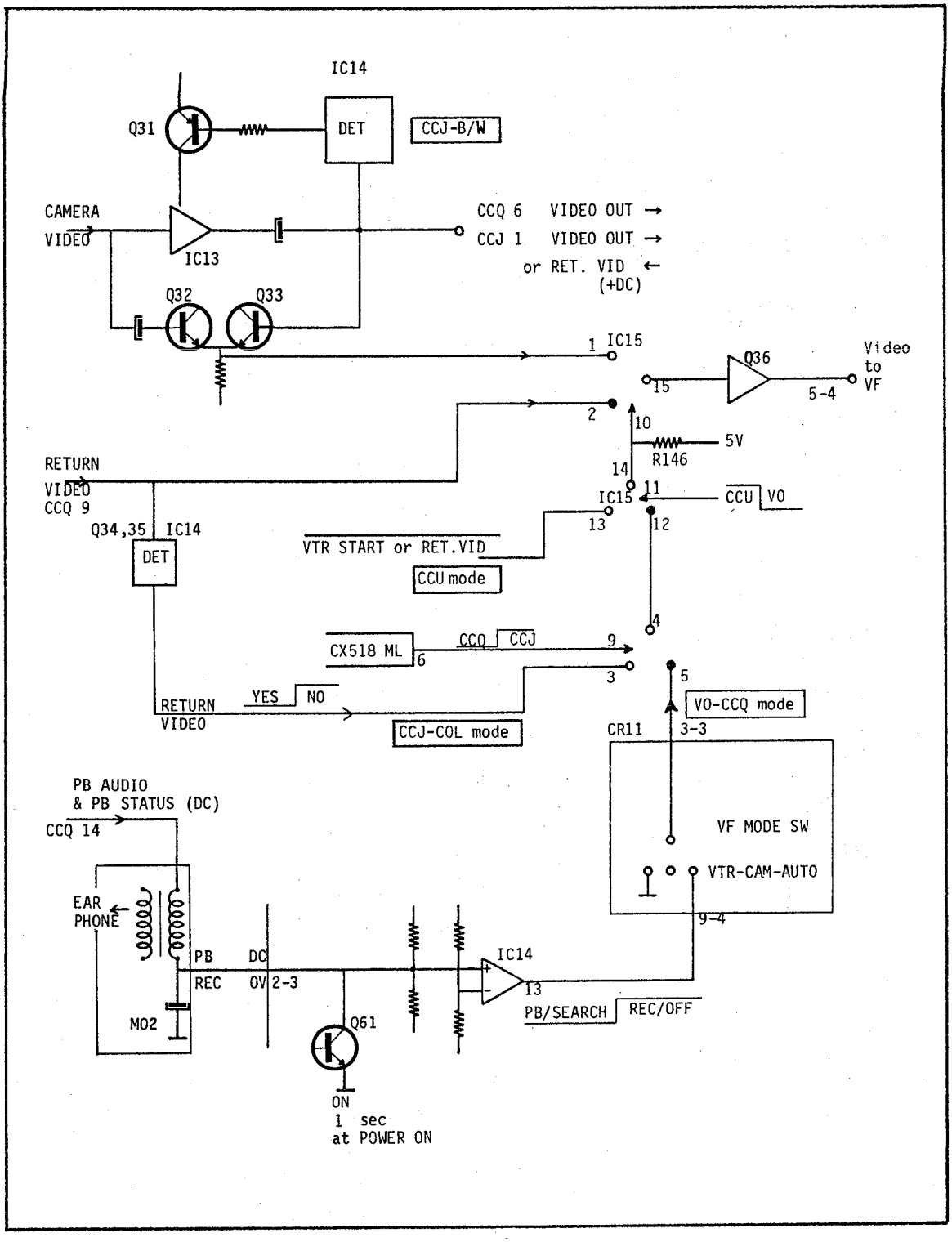


Fig. 10-5. Viewfinder switching in DXC-1800P.

The viewfinder may display the camera or the return video signal. The switch is done by IC15, TC4053. The same IC is also used to perform logical switching functions. Selection depends on which device the DXC180OP is connected to.

In case of the camera control unit, the CCU IND line is High , and the VF switch is controlled through IC15 pins 14 and 13 by the VTR START/ RETURN VIDEO (combining these two in one switch saves place). Note the pull-up resistor R 146.

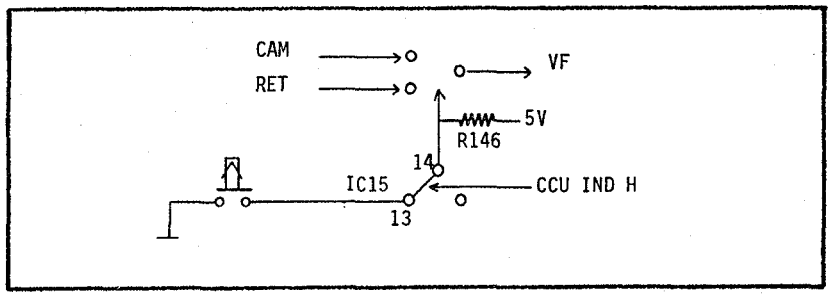


Fig. 10-6. CCU mode.

In case of a VTR or other device with CCJ/10P connector, the selection depends on the presence of return video on pins CCJ1 = CCQ6 and CCJ3 = CCQ9.

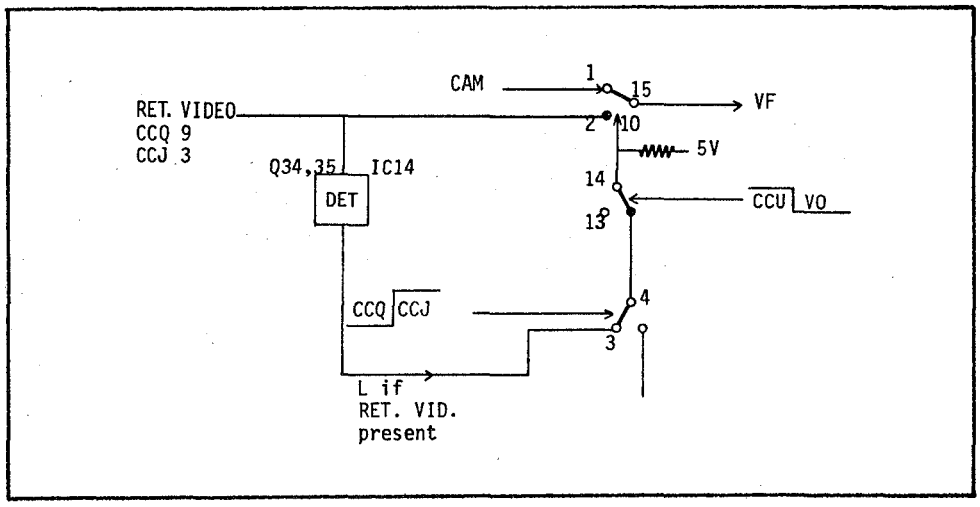


Fig. 10-7. CCJ-COL mode

If return video is present at CCJ3/CCQ9 (VO-3800P is in colour camera mode; DXC-1800P is powered by its own battery), this is detected by Q34,35, IC14. Then IC15 - pin 3 is low and the VF selector is in the bottom position (pins 2 and 15 connected) to display return video.

If there is no return video at CCQ9 then IC15 - 3 is high (open), pin 10 is high and the analog switch remains in position 1-15. (VO-3800P is in B/W camera mode, DXC-1800P is powered from VTR.) Return video is present on CCJ1 / CCQ6, accompanied by a DC voltage. This is detected in IC14 : power to the video output amp is cut-off. The return video with its own DC-bias goes via Q33 to the VF. Q32 is biased lower and therefore cut-off automatically. Without return video at CCJ1, the camera passes through Q32 to the viewfinder.

In case of a CCQ-VTR like the VO-4800PS the VF switch is controlled by the logic signal AT IC15 - 5.

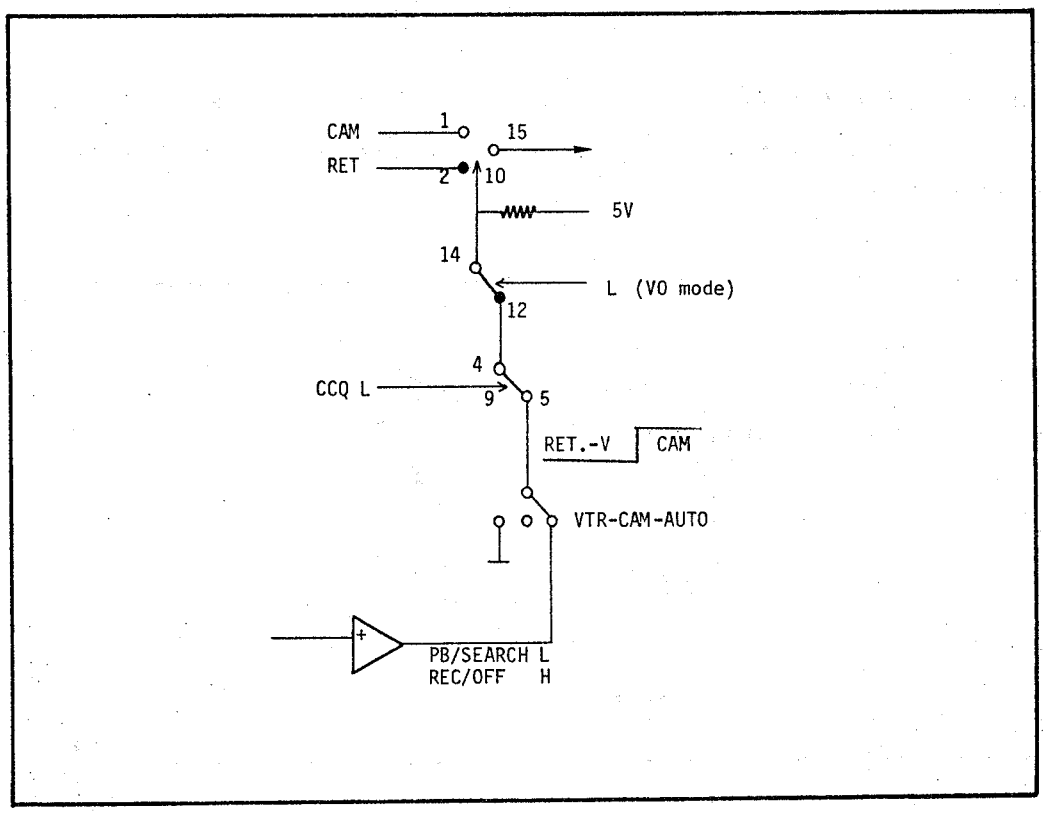


Fig. 10-8. CCQ mode.

This control signal may be fixed L (VTR) or H (CAM) or automatic. In the latter case the VO PB status is recovered from CCQ14 and translated to TTL levels.

11. CCU INTERFACE

All signals go via one standard CCQ cable (same as for connection to VTR) up to a distance of 100m.

This is made possible by the low power consumption of the camera, the combination of gen-lock and return video signals, and the digital data link.

The CCU-1800P itself does not have an AC power supply. Instead the CMA7CE is used which can power the CCU, the DXC and two DXF40 studio viewfinders. See table on page 6 for operating time on batteries.

Part Numbers for connectors :

CCQ(14p) connector,	male	1-508-929-00
	female	1-561-043-00
cable (without connectors)		7-613-091-80
DIN (4p) connector,	male	1-508-723-00
	female	1-508-950-00
cable (without connectors)		7-613-093-60

The CCQ cable contains two 75 coax cables. One carries the camera signal to the CCU, so that only one is a vailable for gen-lock and return video.

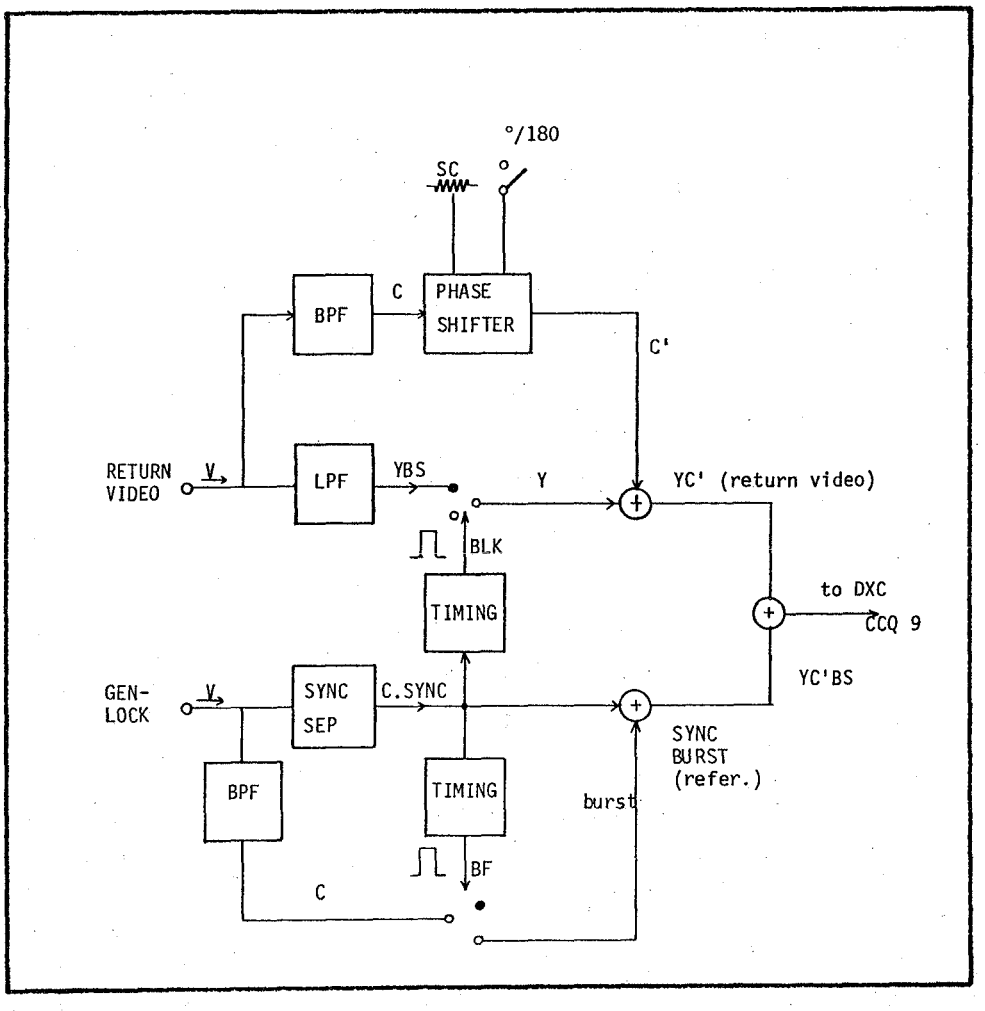


Fig. 11-1. Gen-lock/return video system in the CCU-1800P

So sync and burst are taken from the gen-lock or reference signal while luminance and chrominance are from return video. Reference sync and burst are not processed and pass only the minimum of circuitry. Hor. and SC phase adjustment of the camera signal is done in the camera itself. This can be controlled from the CCU through the digital link.
Chroma phase of the return video signal can be shifted to line it up with the reference burst. This results in correctly phased colour for the return video signal (colour viewfinder).

11-1. µP - Remote control

Following signals can be controlled from the CCU :

analog signals	WB	R	
		B	
	IRIS		
	PEDESTAL		
	CHROMA LEVEL		
	HOR. PHASE		
	ST. PHASE		
logic signals	IRIS	MAN/AUTO	1 bit
	GAIN	AUTO/0/+6/+12	2 bits
	WB	MAN/AUTO	1 bit
	ABL	ON/OFF	1 bit
	C.BARS/CAMERA		1 bit
	SC	0/180°	1 bit

In CCU mode the control buttons and pots on the camera are disabled. (Exception : the W/B switch on the camera is still active. The preset position even overrides the CCU controls.)
The analog signals are controlled (except AUTO - WB) remotely from the CCU through a digital data link. Logical signals select preset or memory (variable) value.

The settings are memorised both in the control unit and in the camera. The CCU-µP scans the inputs. When one of them differs from the stored value (this is done very quickly by only 1 or 2 comparisons), then the new value is converted to digital and transmitted.

The D/A conversion uses the same A/D ladder network and comparator as in the camera head unit.

Following is the format of the serial digital data, which are transmitted via pin 10 of the CCQ cable (battery alarm in VO-mode).

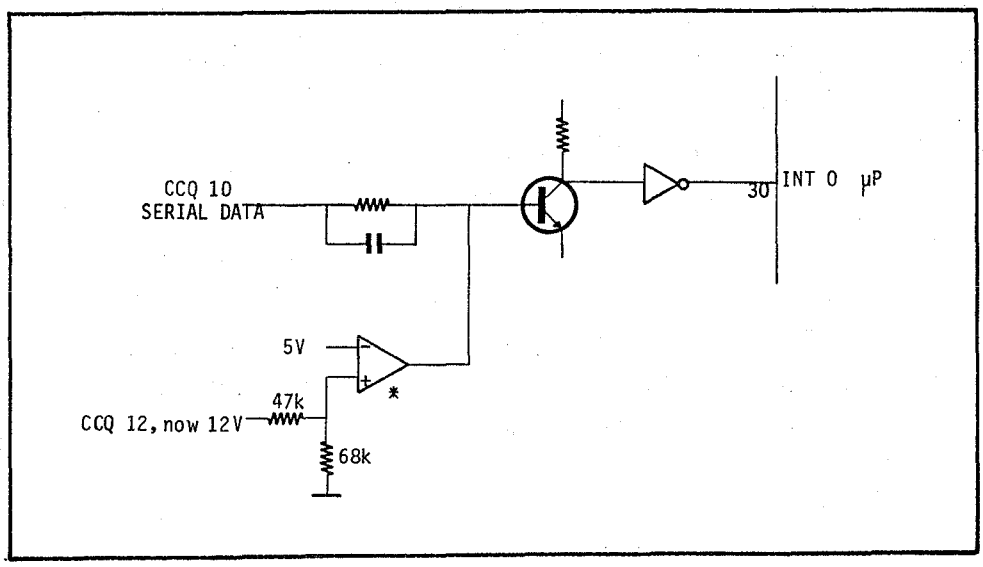


Fig. 11-2. Connection of CCQ10/12 to µP

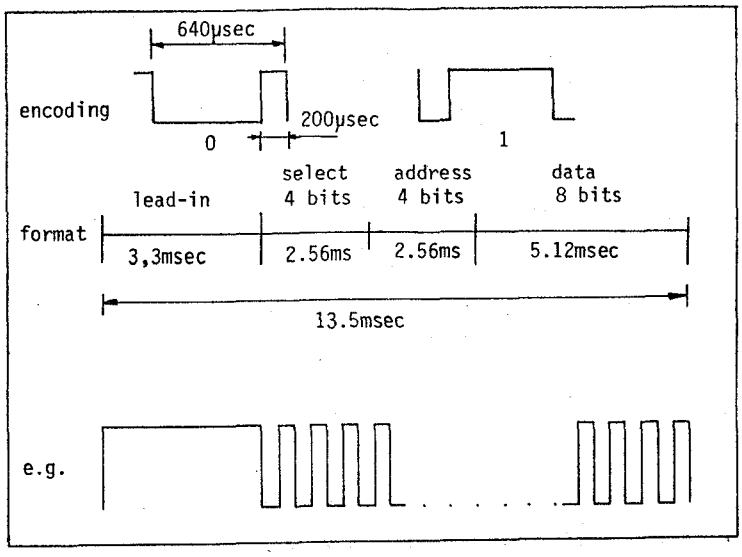


Fig. 11-3. Serial data format.

Via a gate as discussed earlier, the serial data arrive at pin 30 of the microprocessor, which is an interrupt input. This means when INT 0 goes high, the processor stops the current program and jumps to a subroutine to monitor the INT 0 line. By detecting the timing of positive and negative edges the microproprocessor is able to decode the signal. This is a rather inefficient way of data transmission, and is colloquially known as bit banging. However, it is very simple in hardware and quite suitable for this application.

At each burst of data, one analog signal is transmitted. The first 4 bits indicate that an analog signal is sent; the next four are the address, and then follow the 8 data bits.

e.g.

0 0 1 0	0 0 0 0	0 0 1 0	0 1 1 1

Analog signal address codes :

QB R-Y	0 0 0 0
B-Y	0 0 0 1
C level	0 0 1 0
/	0 0 1 1
PEDESTAL	0 1 0 0
HOR.PHASE	0 1 0 1
SC .PHASE	0 1 1 0
IRIS	0 1 1 1

Fig. 11-4.

A. INTRODUCTION TO MICROPROCESSORS

Although many different types of microprocessors are available today, they share many features in common. In fact, as microprocessor designs have evolved over the last several years they have approached more and more closely the ideal of a self-contained "single-chip computer". Such a computer is fabricated as an integrated circuit (IC) on a single chip of silicon. It is able to execute stored programs and is designed to interface easily to external devices.

THE IDEAL MICROPROCESSOR

Letus consider what might be called an "ideal" microprocessor. As shown in Fig. A-1, the ideal microprocessor has N input lines and M output lines. Since the microprocessor is a digital device, only two permissable voltage levels may be applied to any input line. Similarly, only two possible output voltage levels can emerge at any output line. These two voltages are called logic zero and logic one and are symbollically represented by the binary digits (called bits) 0 and 1.

Signals on the input lines are the data input to the microprocessor. These data may come from switches, sensors, analog-to-digital converters, keyboards, or any number of other such devices. Inside this ideal microprocessor resides the microprocessor program. The program is a set of sequential instructions that determine how the input data is to be processed, and what information is to be sent to the output lines as a consequence of this input data. The output lines may be connected to actuators, digital displays, digital-to-analog converters, printers, alarms, or any of a variety of output devices.

Conceptually, then, a microprocessor is a digital device that accepts data from any number of input lines, processes the data according to the dictates of a stored program, and produces any number of output signals as a consequence of this data processing. At any given time, the logic levels on the output lines of a microporcessor are determined by just two factors:

1. The complete history of input signals to the microprocessor up to that time.
2. The stored program of the microprocessor.

The key to the great versatility of the mciroprocessor is that for the same or very similar hardware, programs can be designed for a great number of different applications.

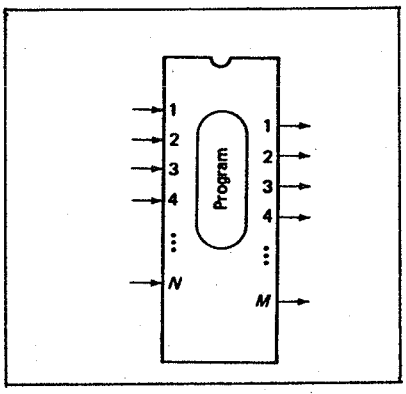


Fig. A-1. The ideal microprocessor

THE DATA BUS

Unlike the ideal microprocessor, real microprocessors cannot afford the luxury of N input lines and M output lines if the numbers N and M are very large. There are a limited number of pins available on any practical IC package. For most microprocessors, N is equal to M. This number is defined as the data path width or word size of the microprocessor. The single most common parameter used in microprocessor taxonomy is the data path width. The lines used to carry data to and from the microprocessor are collectively called the data bus.

Figure A-2a shows an 8-bit microprocessor which has an 8-bit-wide data path (that is, N = M = 8). This microprocessor operates on just 8 bits of data at any one time. A data word of 8 bits is defined as a byte. A compact notation for representing the 8-bit-wide data bus is shown in Fig. A-2b. A 4-bit microprocessor is illustrated in Fig. A-3. A 4-bit data word is defined as a nybble.

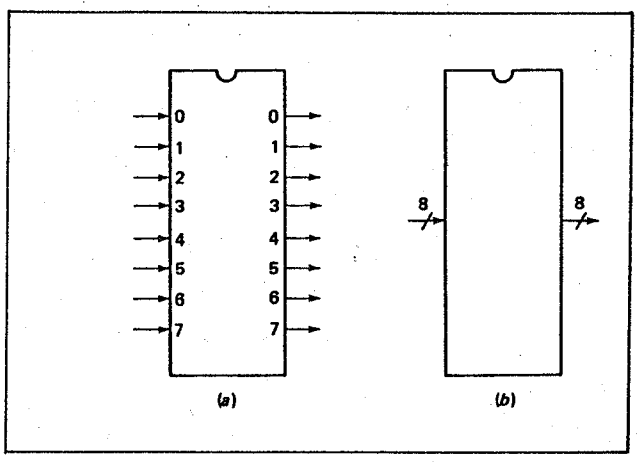


Fig. A-2. The 8-bit microprocessor. Each data word contains 8 bits or 1 byte

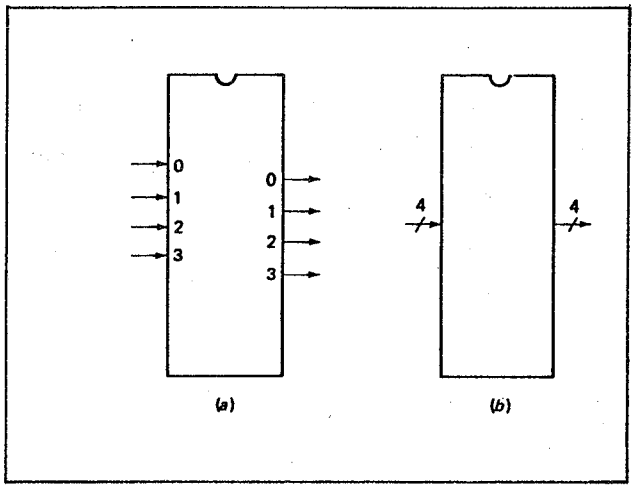


Fig. A-3. The 4-bit microprocessor. Each data word contains 4 bits or 1 nybble.

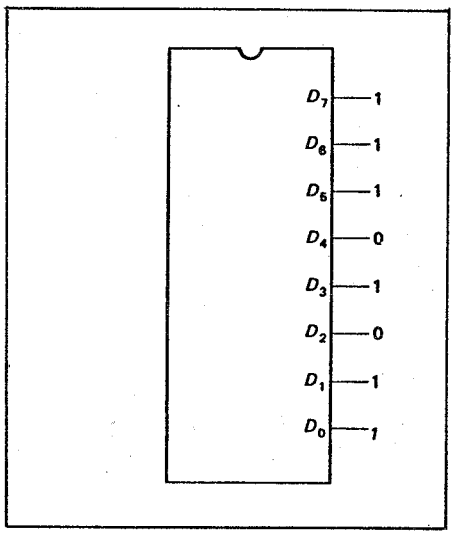


Fig. A-4. An 8-bit microprocessor data bus. D7 is the most-significant bit (MSB) and D0 is the least-significant bit (LSB).

At any given time, the logic levels on the data lines of a microprocessor define a specific data word. For the case of the 8-bit microprocessor shown in Fig. A-4, the data word is made up of the eight binary digits D0 through D7. D0 is called the least-significant bit or LSB. D7 is called the most-significant bit of MSB. The data word on the data bus can be numerically represented in several different ways. The simplest way is in binary notation as a binary number. In this notation, the 8-bit data word shown in Fig. A-4 is written as 11101011. To show that this is a binary number it can be suffixed by the letter B or the subscript 2 as shown:

$$11101011B \text{ or } 11101011_2$$

This data word could also be represented as an octal number. In octal notation, each group of three binary digits is assigned a single number between zero and seven according to Table 1-1.

Binary number	Octal digit
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

Table A-1. The octal digits

This table can be used to find the octal equivalent for the binary word:

```
11 101 011     binary
 3   5   3     octal
```

353 is the octal equivalent of the binary number 11101011. To show that the number is in octal notation it can be suffixed with the letter Q or the subscript 8 as shown:

$$353Q \quad \text{or} \quad 353_8$$

A third way to represent the data word (and the way most commonly used with microprocessors) is as a hexadecimal number. In hexadecimal notation, each group of 4 bits is assigned a single character according to Table A-2. The hexadecimal equivalent for the binary number above can be found as follows:

Binary number	Hexadecimal digit
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F
1110 1011	binary
E B	hexadecimal

Table A-2. The Hexadecimal digits

EB is the hexadecimal equivalent of the binary number 11101011 and the octal number 353. The word "hexadecimal" is commonly abbreviated simply as hex. A hex number can be suffixed with the letter H or the subscript 16 to show that it is written in hexadecimal notation:

EBH or EB_{16}

One of the most severe practical limitations of the microprocessors is the limited number of pins available in an economical IC package. To save on the number of pins required, many microprocessors use the same pins for both input data bus and the output data bus. At any given time, the pins are used either for input or output but are never used for both simultaneously. Fig. A-5 diagramatically shows a 4-bit microprocessor with a bidirectional data bus. Fig. A-5a shows the data bus in the input mode and Fig. A-5b shows the bus in the output mode.

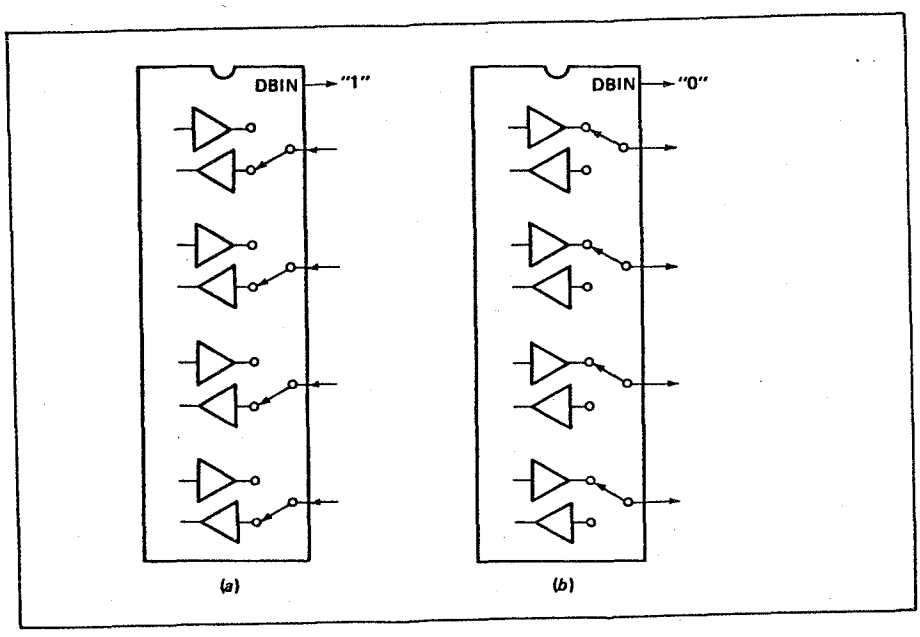


Fig. A-5. A 4-bit microprocessor showing the operation of the bidirectional data bus (a) Data bus in the input mode.
(b) Data bus in the output mode.

Fig. A-5 also shows a special control output of the microprocessor, DBIN in this case, that is used to indicate to external circuitry whether the data bus is in the input mode or the output mode. DBIN goes high (logic 1) to indicate the input mode and goes low (logic 0) to indicate the output mode.

The notation for representing the bidirectional data bus of an N-bit microprocessor is shown in Fig. A-6.

THE ADDRESS BUS

For the ideal microprocessor, the output data can be a function of the total history of the input data. The nature of this function is determined by the microprocessor program. While the ideal microprocessor is assumed to have an unlimited internal memory, real microprocessors are necessarily limited in the amount of internal memory available for data and program storage. As a result, the microprocessor very often must have access to an external memory. In general, the microprocessor must be able to both store information in this memory and retrieve information from it. The process of storing information in memory is called memory writing. The process of retrieving information from memory is called memory reading.

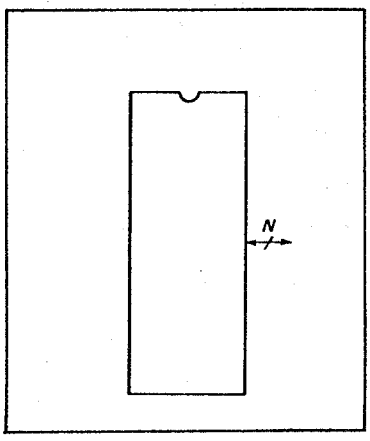


Fig. A-6. An N-bit microprocessor with a bidirectional data bus.

Information is stored in memory at a set of memory locations. Each memory location contains one word of memory. The size of the memory word is determined by the data path width of the microprocessor. An 8-bit microprocessor, for example, requires each memory location to contain an 8-bit data word or byte. A different memory organization would be used for a 4-bit microprocessor, however, so that each memory location contained a 4-bit word or nybble.

Each location in memory has a unique memory address. Unless otherwise stated, this address will be specified using hexadecimal notation.

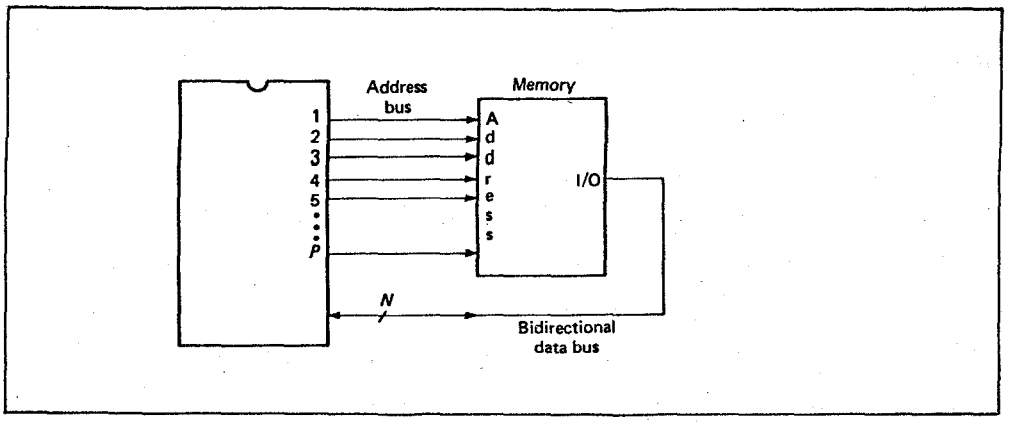


Fig. A-7. The address bus is used to select memory locations in external memory

Before reading or writing at a memory location, the microprocessor must first select the desired memory address. Some microprocessors output this information on the data bus just prior to any memory read or write operation. Most microprocessors, however, have a separate address bus as shown in Fig. A-7. Each line of the address bus can be either at logic 1 or at logic 0. Since each line has just two states, a microprocessor with P address lines is able to address 2P unique memory locations. Table A-3 shows the evaluation of 2^P for values of P ranging from 0 to 20.

P	2^P	P	2^P
0	1	11	2048
1	2	12	4096
2	4	13	8192
3	8	14	16384
4	16	15	32768
5	32	16	65536
6	64	17	131072
7	128	18	262144
8	256	19	524288
9	512	20	1048576

Table A-3. The Powers of 2

THE CONTROL BUS

In addition to the data bus and the address bus, microprocessors must also have a set of control lines - both input control lines and output control lines - that can be used to synchronize the operation of the microprocessor to the operation of external circuitry. Collectively, these control lines are the control bus of the microprocessor. You have already seen one example of a control output line, namely the DBIN signal of Fig. A-5. This signal is used to indicate to external circuitry the status of the microprocessor bidirectional data bus.

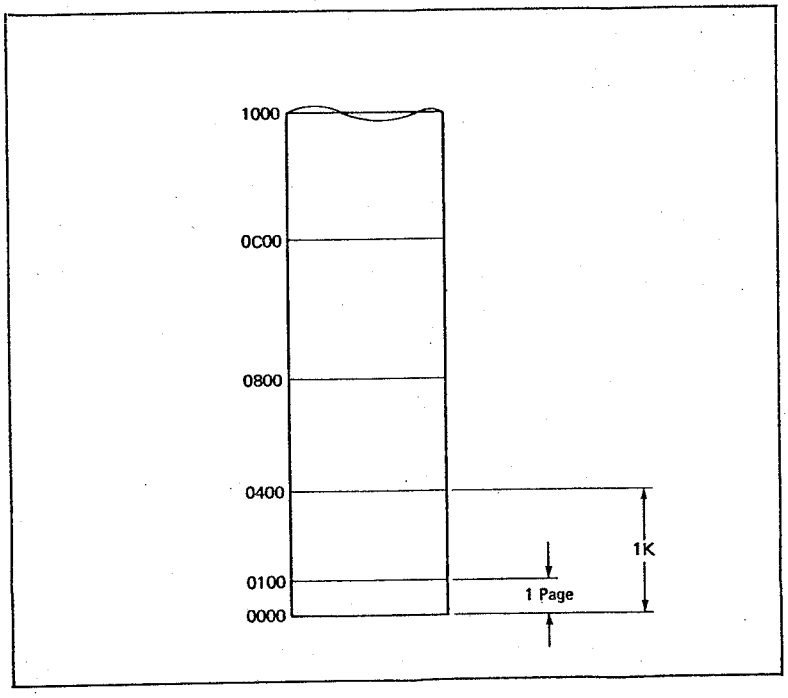


Fig. A-8. The 1K boundaries of memory are shown here for the first 4K of memory space. There are four pages of memory in every 1K of memory space.

As another example of where control lines are required, suppose that some external device needs to directly access the memory of a microprocessor system. In order to accomplish this direct memory access or DMA, there must exist some mechanism for effectively disconnecting the microprocessor from its memory so that the external device can gain control of the address bus and the data bus.

A special control input is provided on many microprocessors to permit DMA operation. This input is labelled HOLD in Fig. A-9. A logic 1 signal on the HOLD line indicates to the microprocessor that some external device is requesting control of the address and data buses. In order to accommodate this request, the microprocessor places its address and data bus outputs in what is called a tristate condition, shown diagrammatically in Fig. A-10.

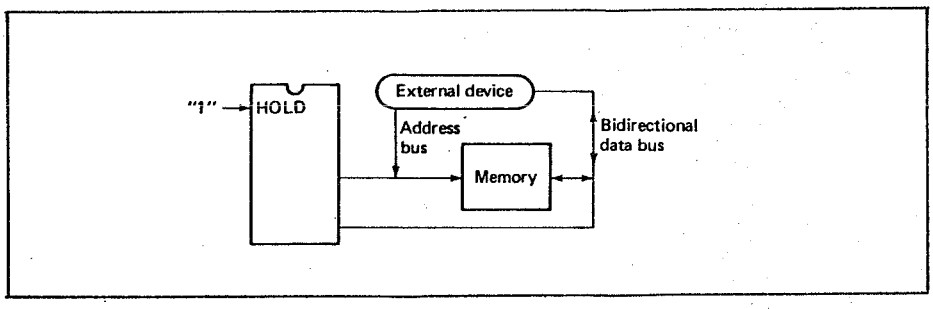


Fig. A-9. Direct memory access by an external device

This effectively disconnects the microprocessor from the address and data buses.
Once the address and data bus outputs enter this tristate condition, the microprocessor in this example responds to the external device's HOLD request by issuing a hold acknowledge signal on the HLDA line shown in Fig. A-10. HLDA is another example of a typical control output line of a microprocessor control bus. The external device is designed to wait for a logic 1 signal on the HLDA line before actually taking over the address and data bus. This communications protocol of making a request and then waiting for a response before proceeding is called handshaking. Handshaking protocols like this are very common in microprocessor systems.

Any given control signal of a control bus can be either active high or active low. In the case of the examples discussed above (DBIN, HOLD and HLDA), the signals are said to be active high because a logic 1 is used to indicate the active signal condition. If, for example, a logic 0 indicated that the data bus was in the input mode, then a bar would be placed over the signal name to indicate that it was in

fact an active low signal. If this were the case, the control output would be labelled $\overline{DBIN}$ which is pronounced "dee bee in bar". The bar notation is very convenient for showing at a glance which control signals are active high and which are active low.

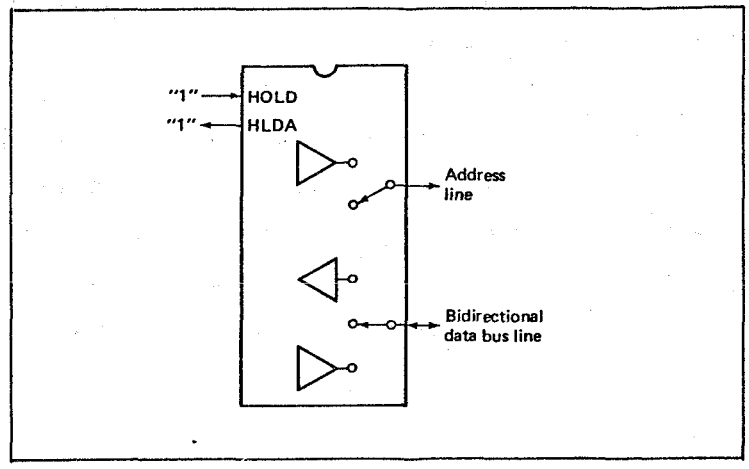


Fig. A-10. An address line and bidirectional data bus line shown in the tristate condition when a logic 1 signal is applied to the HOLD input of the microprocessor.

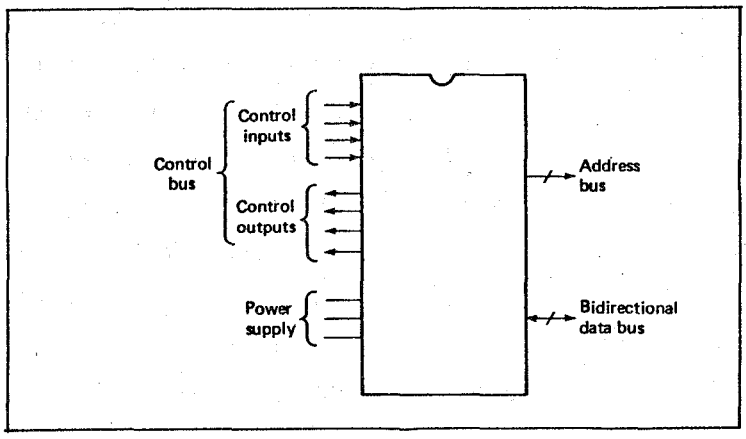


Fig. A-11. The generalized microprocessor.

THE GENERAL MICROPROCESSOR

We are now prepared to formulate a generalized model of a microprocessor. As shown in Fig. A-11. the microprocessor is a digital device with (1) a data bus, (2) an address bus, and (3) a control bus. The microprocessor is able to input information in the form of digital signals, process information according to a stored program, and output information in the form of digital signals. The stored program may in some cases reside in memory internal to the microprocessor itself. In other cases the program may be stored in external memory. In addition to the three major buses, the microprocessor requires one or more power-supply voltages to power its internal circuitry and provide a voltage reference for the microprocessor signal lines.

B. MICROPROCESSOR EVOLUTION

Since the introduction of the first microprocessor in 1971, microprocessor performance has increased impressively. Improved performance has been achieved in three ways. First, more advanced technologies have been employed in microprocessor fabrication. Second, the detailed logic design or architecture of the microprocessor has improved. And third, more memory and I/O interfaces have been included on the microprocessor chip itself, thus reducing the required number of external components. In brief, microprocessors are evolving toward the ideal microprocessor described in Chap. 1: a device with only inputs, outputs, and a resident program.

Of course, the ideal microprocessor will only be approached asymptotically. An engineer designs with real devices. For microprocessors, this means you must learn hardware design - the physical implementation of external circuitry required to take full advantage of the microprocessor - as well as software design - the formulation of the detailed steps of the microprocessor program. As microprocessors have evolved, both hardware and software design have actually become easier to implement for systems with

comparable capabilities.

To see how microprocessors have evolved, six specific examples of microprocessors will be discussed in this chapter: the 8008, 8080, Z80, 8748, Z8000, and 8086. The 8008 and 8080 are 8-bit microprocessors discussed primarily for historical perspective. The Z80 and 8748 are current 8-bit microprocessors. The Z8000 and the 8086 herald the beginning of high performance 16-bit microprocessors. Detailed information on each of these microprocessors can be found in the manufacturers' literature cited at the end of this chapter.

The 80008 is an 8-bit, first-generation microprocessor that was introduced in January 1972. It is actually the second of the first-generation processors, following the 4004, a 4-bit processor introduced in November 1971. The 8008 is fabricated using the P-channel MOS process, and is compact as microprocessors go, being packaged in an 18-pin dual in-line package (DIP). The pinout is shown in Fig. B-1.

Referring to Fig. B-1, we see that eight pins of the microprocessor are used as an 8-bit bidirectional data bus. Two power-supply voltages are required: V_{DD} is -9 V and V_{CC} is +5 V. Two clock signals, Ø1 and Ø2 are also required. Three lines of the microprocessor (S0, S1 and S2) are used to indicate the state of the microprocessor to external circuitry. The SYNC output is used to indicate the beginning of each machine cycle when new information is put out on the state lines. An important feature of the 8008 is the READY line which can be used to temporarily stop the operation of the microprocessor by applying a logic 0 signal to this input. Finally, the 8008 has an interrupt input that can be used to change the course of execution of the microprocessor program. External hardware can be used to put a logic 1 signal on this input to effect an interrupt. A summary of the 8008 pinout is shown in Fig. B-2.

The 8008 has no provision for program storage on the microprocessor chip itself. The microprocessor program must be stored in memory external to the microprocessor, which can be addressed and read by the microprocessor.

But the 8008 has no address lines. How can this be?

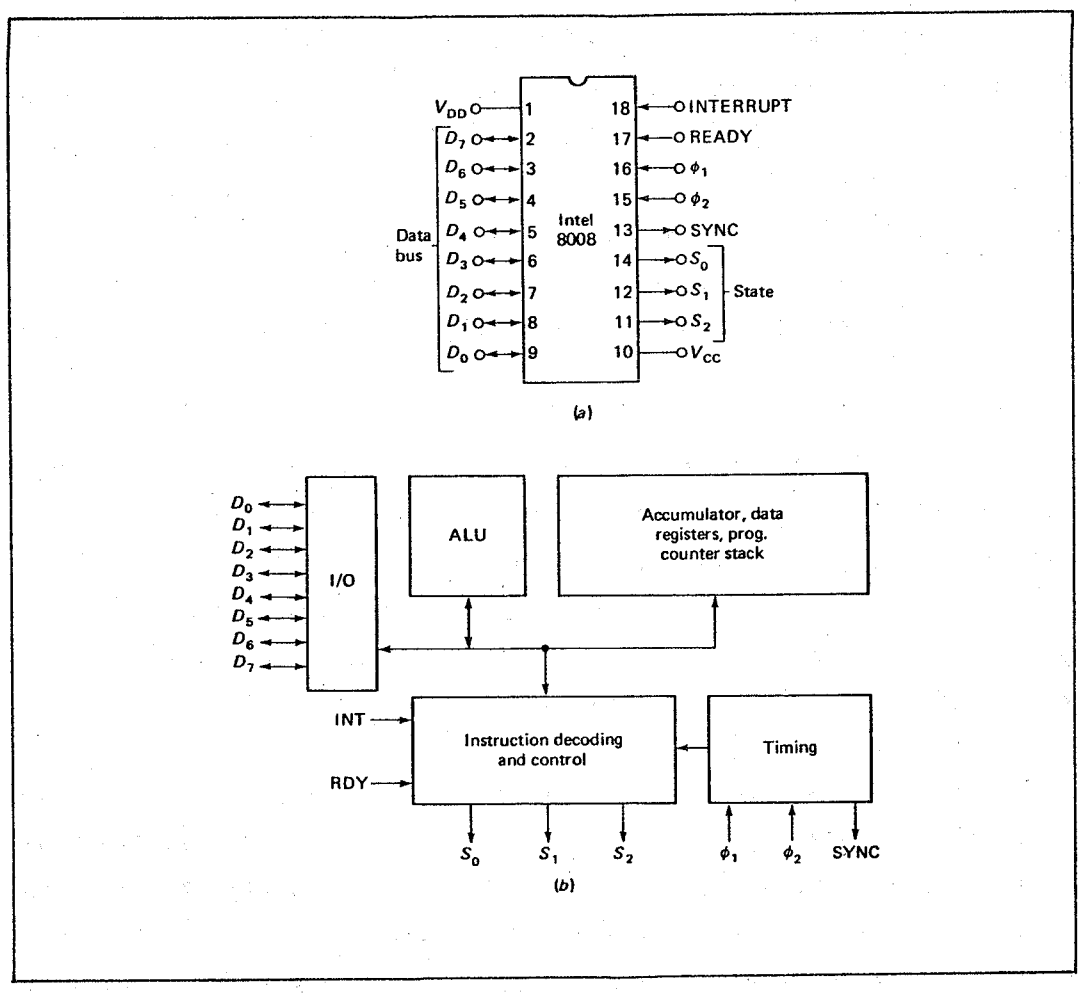


Fig. B-1. (a) Pin configuration. (b) Block diagram

Quite simply, address information (the coded sequence of bits used to select an external memory location) is multiplexed on the 8-bit bidirectional data bus. At the beginning of each cycle requiring a memory reference (either to read from or write to memory), address information is put on the "data" bus at the beginning of the machine cycle. This address information must be saved or latched by external circuitry. Only then does the actual data transfer occur on the data bus. The address put out by the 8008 is 14 bits long. First, the eight low-order bits are put out and externally latched. Then, the six high-order bits are put out and externally latched. The 8008 is thus able to address 2^{14} or 16,384 separate memory locations.

The architecture of the 8008 is shown in Fig. B-3. Although it is not necessary to understand this diagram in complete detail at this time, several points should be mentioned. First, note that there is memory space on the chip that can be used for data storage (although not for program storage). This memory space is organized as seven 8-bit registers (registers A, B, C, D, E, H, and L). The contents of these registers may be modified or interrogated by the microprocessor program. The A register is also called the accumulator since the result of arithmetic operations is normally stored here. Also note that the 8008 has eight internal 14-bit storage locations. One of these is called the program counter (PC) and is used to store the address of the instruction in external memory that is currently being executed by the microprocessor. The remaining seven 14-bit locations comprise what is called the stack. If during the course of the microprocessor program, a subroutine call instruction is encountered, the current value of the program counter is stored in the stack to save the return location before the processor branches to the subroutine. Since there are seven stack locations, there can be a maximum of just seven nested subroutines in an 8008 program.

Address	Data	Control bus		Power Supply, V
		Inputs	Outputs	
14 bits multiplexed on data bus	8-bit bidirectional	Interrupt Ready Ø1 Ø2	Sync S0 S1 S2	+5 -9

Fig. B-2. Summary of 8008 pinout

One measure of performance of a microprocessor is the number of different program instructions in its repertoire. The number of instructions in its instruction set is one measure of the power of the instruction set. For the case of the 8008 there are a total of 48 distinct instructions that comprise the instruction set.

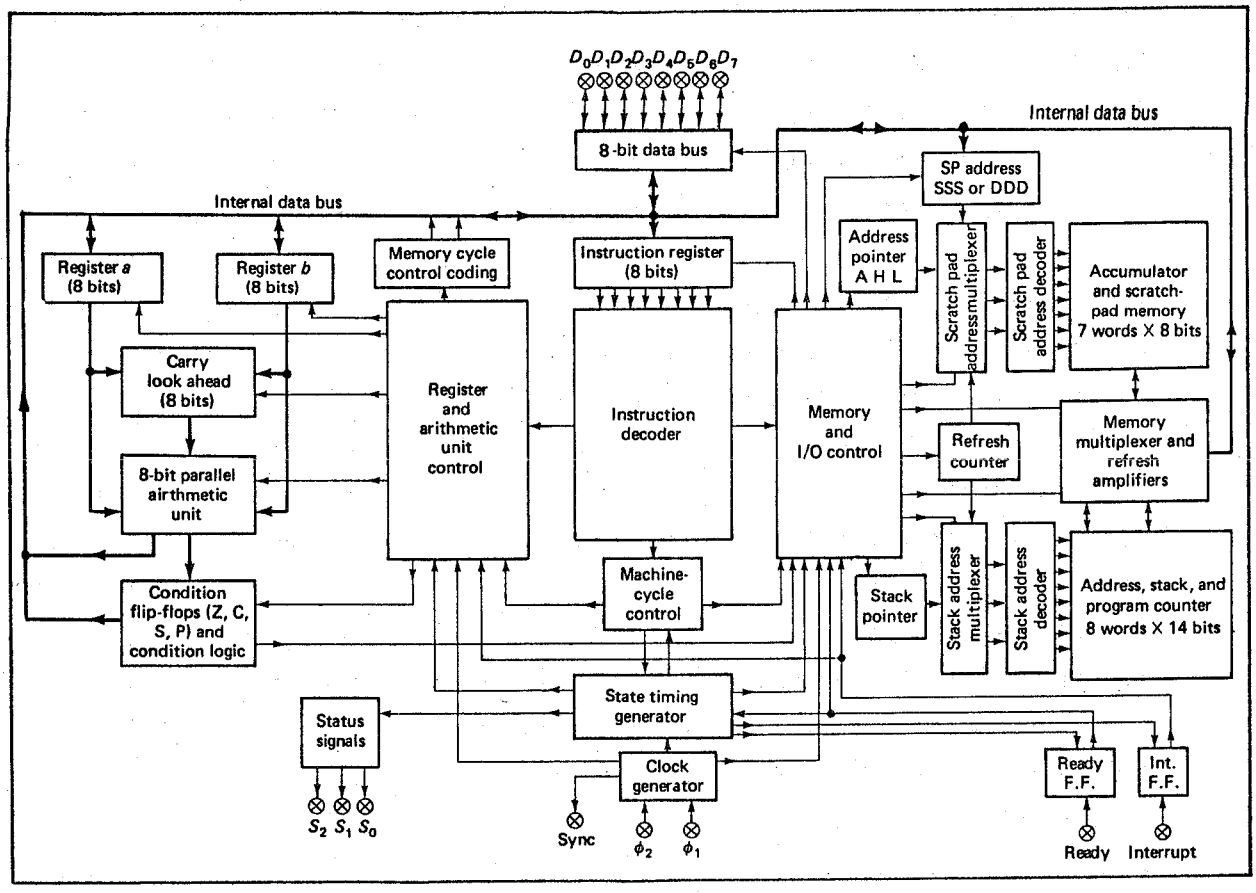


Fig. B-3. 8008 architecture

The 8008 is a very low-cost microprocessor, but the low cost is achieved at the expense of performance. The P-channel technology is inherently slower than other technologies. And multiplexing address information on the data bus, rather than having separate address lines, slows performance even further. The minimum time required to execute a single program instruction with the standard 8008 is 20μS.

THE 8080

The 8080 was the first of the second-generation microprocessors, and was introduced in November 1973. Today, it is one of the most widely used microprocessors in the world. The 8080 is fabricated using the N-channel MOS process. It is packaged in a 40-pin DIL as shown in Fig. B-4. The functions of these pins can be divided into five categories:

1. address bus
2. bidirectional data bus
3. power supply
4. control bus inputs
5. control bus outputs

The 8080 has 16 address lines and is thus able to address up to 2^{16} or 65,536 bytes of memory. The 8080 also has an 8-bit bidirectional data bus.

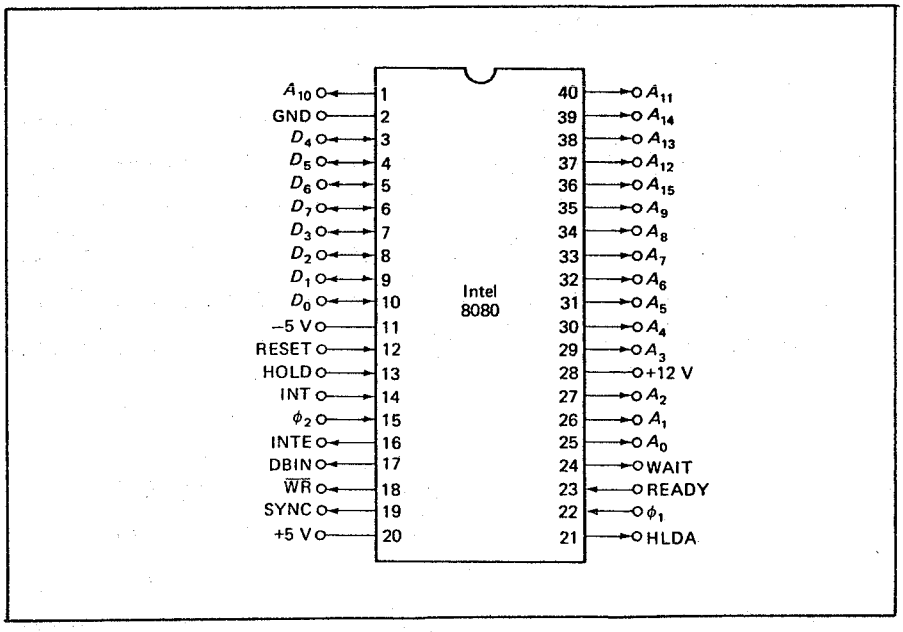


Fig. B-4. 8080 pin configuration.

The DBIN output (pin 17) is used to signal whether the data bus is in the input mode (DBIN = 1) or the output mode (DBIN = 0). Three power supply voltages are required: +12V at 40mA, +5V at 60mA, and -5V at 10mA. All power-supply voltages are with reference to ground (pin 2). Six pins of the 8080 are used as control inputs. There are two clock inputs, the HOLD input, the READY input, the interrupt request (NT) input, and the RESET input.

Two clock signals, Ø1 (pin 22) and Ø2 (pin 15), are required by the 8080 for internal sequencing and timing. These two clock signals are nonoverlapping. 12-V pulse trains that must meet specific timing requirements.

The HOLD input (pin 13) is held at logic 0 during normal operation of the 8080 microprocessor. To perform direct memory access (DMA), the HOLD input is raised to a logic 1 level to request that the processor enter a hold state. In the hold state, the processor ceases activity, and the data and address lines are in their high-impedance (tristate) mode.

The READY input (pin 23) is held at logic 1 during normal operation of the 8080. A logic 0 signal is applied to this input to request that the processor enter a wait state. Once in the wait state, the processor ceases activity until the READY input returns to logic 1.

One use of the READY input is in synchronizing the 8080 with slow memory or peripheral devices. After an address is put out on the address bus prior to a memory read, for example, the 8080 interrogates the READY line to see if the memory is prepared to respond with the desired byte of data. For the case of memories with slow access times, READY will be held low at this point, and continue to be held low, until valid data are on the data bus.

One difference between the hold state and the wait state is that the hold state can only be entered following the completion of an instruction of the microprocessor program. The wait state, on the other hand, is entered during the middle of an instruction execution, just after new address information is put on the address bus. A second difference is that in the hold state, the data bus and address bus are in their tristate mode while in the wait state they are not.

The interrupt request input is pin 14. While the 8080 is executing a program, it is possible to interrupt the program execution and branch to a new program. This interruption of program execution is initiated by a logic 1 signal on the interrupt request (INT) input. The 8080 will not acknowledge an interrupt request while in the hold state. It will also not acknowledge an interrupt unless its internal interrupt enable (NTE) flip-flop is set. This flip-flop can be set and reset by the program that the 8080 executes.

The RESET input is pin 12. During program execution, the RESET input to the 8080 is held at logic 0. To reset the 8080, and to begin program execution at location 0000H in memory, the RESET input must be held at logic 1 for at least three clock cycles. Program execution begins at location 0000H when the signal to the RESET input returns to logic 0. The interrupt enable and hold-acknowledge (HLDA) flip-flops (described below) are also reset.

The 8080 control bus has six outputs: DBIN, INTE, SYNC, $\overline{WR}$, WAIT, and HLDA. The DBIN output is pin 17 and is used to signal to external circuitry that the 8-bit bidirectional data bus is either in the input mode (DBIN = 1) or in the output mode (DBIN = 0).

The interrupt enable (INTE) output, pin 16, indicates the state of the internal interrupt enable flip-flop. This flip-flop may be set or reset by the enable interrupt or disable interrupt instructions of the microprocessor program. When INTE = 0, the microprocessor will not acknowledge an interrupt request input.

The SYNC output is pin 19. One use of the bidirectional data bus of the 8080 is to output status information at the beginning of each machine cycle. The SYNC pulse appears at the beginning of each machine cycle and is used to indicate the presence of status information on the data bus.

The write ($\overline{WR}$) output is pin 18. The signal is used to indicate when valid output data is available on the data bus. When data is output to external memory or to an output device, the $\overline{WR}$ line goes from $\overline{WR}$ = 1 to $\overline{WR}$ = 0 when the output is valid.

The WAIT output is pin 24 and is used to indicate when the processor is in a wait state. WAIT = 1 when the processor is in a wait state; otherwise, WAIT = 0. There are two ways by which the wait state can be requested. One way is by applying a logic 0 signal to the READY input. The second way is by execution of the HALT instruction in the microprocessor program.

Address	Data	Control bus		Power supply, V
		Inputs	Outputs	
16 lines	8 bidirectional	Ø1	DBIN	+5
		Ø2	INTE	+12
		HOLD	SYNC	-5
		READY	$\overline{WR}$	
		INT	WAIT	
		RESET	HLDA	

Fig. B-5. Summary of 8080 pinout.

The hold acknowledge (HLDA) output is pin 21 and goes to logic 1 to indicate lines and address lines will subsequently go to their high-impedance state.

A summary of the 8080 pinout is shown in Fig. B-5.

In addition to the six output control lines emanating from the 8080 microprocessor itself, eight additional bits of control information are output on the data bus at the beginning of each machine cycle. This is the status information that is used as follows:

D0: INTA, or interrupt acknowledge, indicates that the processor has responded to an interrupt, on the INT control line.

D1: WO indicates by a logic 0 that the processor is in a memory write or an output cycle.

D2: STACK indicates that the processor is doing either a stack read or write operation.

D3: HLTA, or hold acknowledge, signifies that the processor has come to a stop as a result of executing a HALT instruction

D4: OUT indicates that data is being ouput to an output port

D5: M1 indicates that the processor is doing an op code (instruction) fetch from memory.

D6: INP indicates that data is being input from an input port.

D7: MEMR signifies a memory read operation

Even a minimal 8080 microprocessor system requires an external status latch to store this status information at the beginning of each machine cycle.

The architecture of the 8080 is shown in Fig. B-6. Like the 8008, there are seven 8-bit registers (including the accumulator). There is a 16-bit program counter (compared to a 14-bit PC in the 8008). But where is the stack?
Unlike the 8008, the 8080 uses an external stack rather than an internal stack. A 16-bit register, called the stack pointer (SP), keeps track of the location of the stack in external memory. A key advantage of this technique is that the size of the stack is not limited by the number of stack locations on the microprocessor chip itself.

The 8080 also has a more powerful instruction set that the 8008 with a total of 78 instructions. These 78 instructions include the 46 used in the 8008. By using N-channel technology and separate address lines, the 8080 instruction time (for the standard 8080) is 2μS: a factor of ten faster than the 8008.

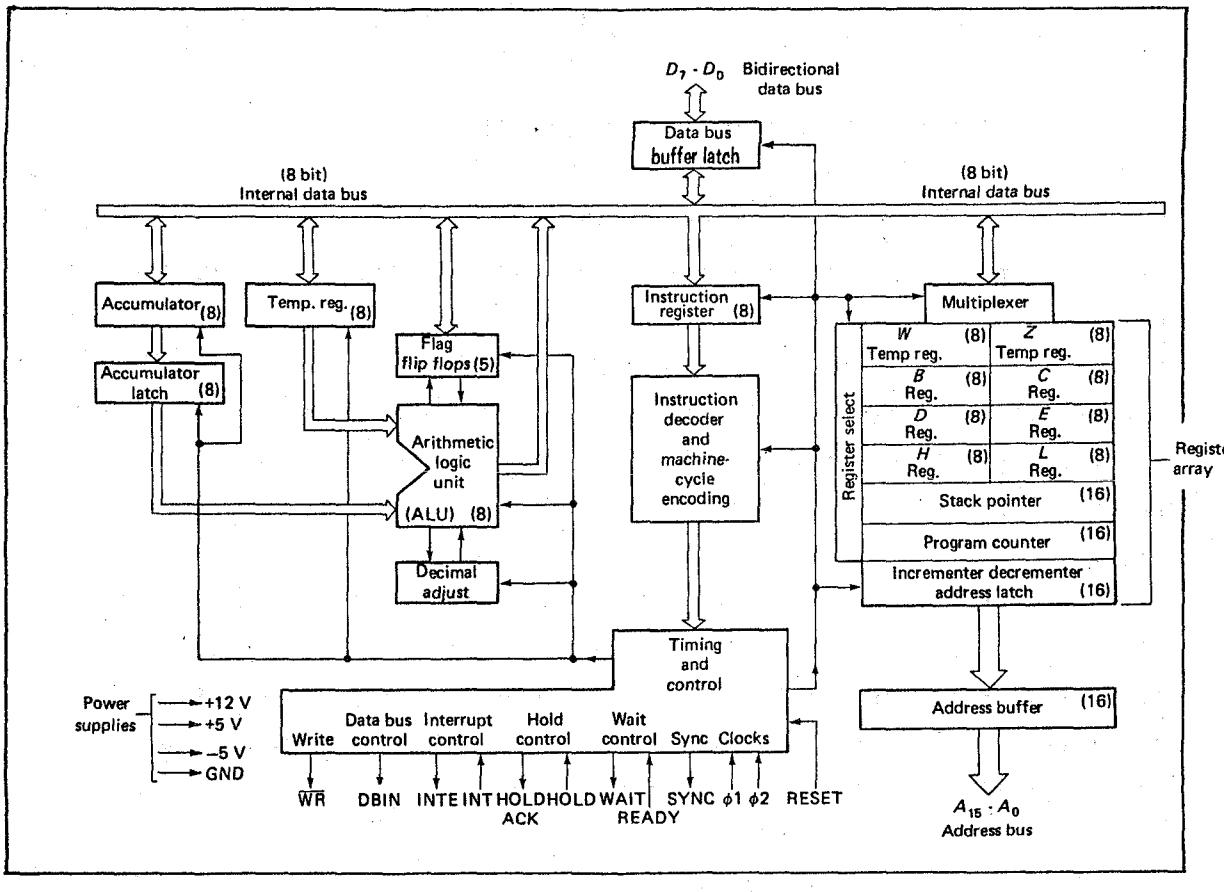


Fig. B-6. 8080 architecture

THE Z80

The first of the third-generation microprocessors is the Z80, introduced in April 1976. By using depletion-mode load, N-channel MOS fabrication, only a single +5-V power supply is required for the microprocessor. Only a single +5-V power supply is required for the microprocessor. Only a single +5-V external clock signal is required. Additional control output signals are generated by the Z80 which eliminate the need to multiplex status information on the data bus, as is done with the 8080. The Z80 is contained in the same style 40-pin DIP that is used for the 8080. The pinout is shown in Fig. B-7. Again, each terminal of the microprocessor can be categorized into one of five categories.

The Z80 has 16 addresses, and, like the 8080, is able to address 64K of memory. The Z80 also has an 8-bit bidirectional data bus. But, unlike the standard 8080, the Z80 requires just a single +5-V supply (pin 11) with respect to ground (pin 29). The Z80 can use a single supply in this way because of the depletion-mode load technology used to fabricate the IC.

The Z80 has six control inputs. These are the clock input (pin 6), the interrupt request input (pin 17), the wait request input (pin 24), the bus request input (pin 25), and the reset input (pin 26).

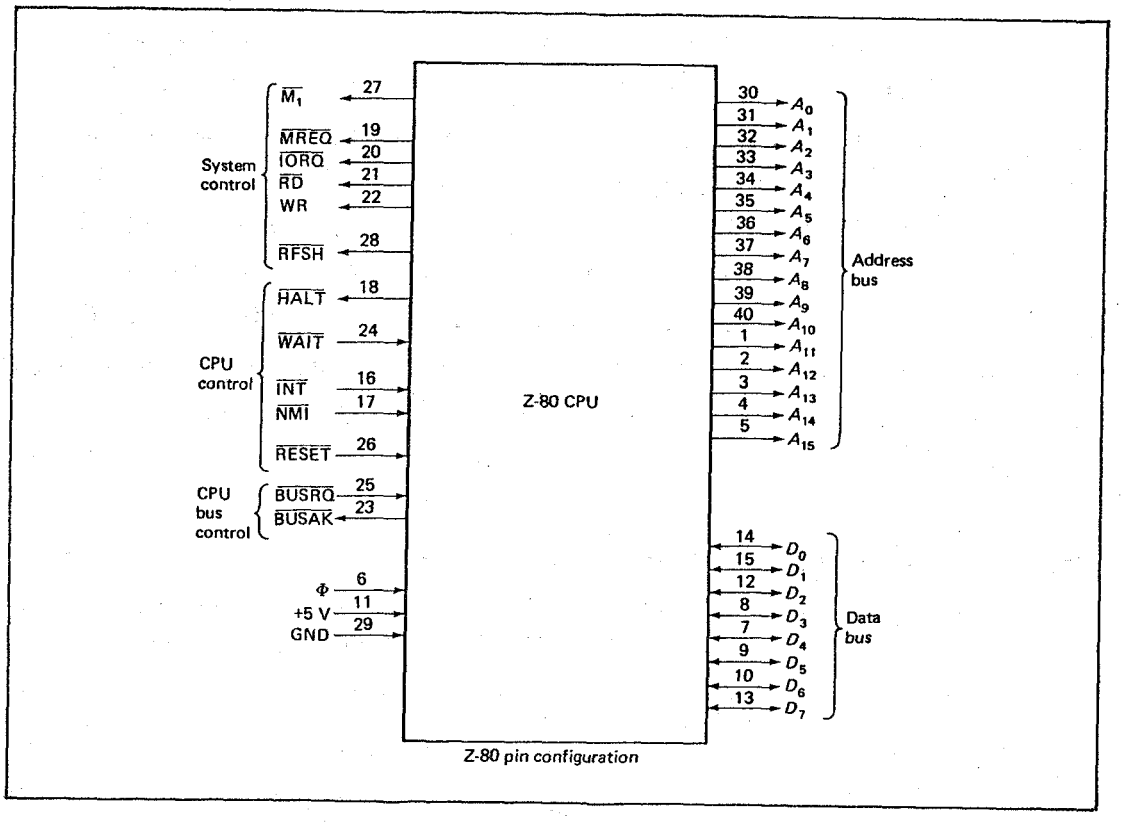


Fig. B-7. Z80 pin configuration

The clock input requires a single 5-V pulse train. The detailed timing requirements are dependent upon the specific mode of Z80 used (e.g., the high-speed or low-speed version) and can be found in the manufacturer's specification sheet. The interrupt request ($\overline{NT}$) is analogous to the INT line of the 8080 except that the request is initiated by an active low (logic 0) signal. This is indicated by the bar over the abbreviation for the input, that is, $\overline{INT}$ (pronounced interrupt bar). The nonmaskable interrupt (NM) is similar to INT except that this input cannot be disabled by software instructions. The $\overline{WAIT}$ request is analogous to the READY line of the 8080. The bus request ($\overline{BUSRQ}$) is analogous to the HOLD like to the 8080. The $\overline{RESET}$ input is analogous to the RESET input of the 8080. Again this input is active low.

The Z80 has eight control output lines. The $\overline{HALT}$ output (pin 18) is analogous to the WAIT output of the 8080. The $\overline{MREQ}$ output (pin 19) goes low (as indicated by the bar) to signal that the address bus holds a valid address for a memory read or write operation. The $\overline{IORQ}$ output (pin 20) goes low to signal that the address bus holds a valid address for a I/O read or write operation. RD (pin 21) goes low to signal a memory or I/O read operation. $\overline{WR}$ (pin 22) goes low to signal a memory or I/O write operation. The $\overline{BUSAK}$ signal (pin 23) is analogous to the HLDA signal of the 8080. $\overline{MI}$ (pin 27) is used to indicate that the current machine cycle is the op code fetch cycle of an instruction execution. The $\overline{RFSH}$ (refresh bar) output (pin 28) has no counterpart in the 8080. This output is used as a control signal to simplify the refresh circuitry required with dynamic memory.

A summary of the Z80 pinout is shown in Fig. B-8.

Address	Data	Control bus		Power supply, V
		Inputs	Outputs	
16 lines	8-bit bidirectional	CLOCK	$\overline{HALT}$	
		$\overline{INT}$	$\overline{MREQ}$	
		$\overline{NMI}$	$\overline{IORQ}$	
		$\overline{WAIT}$	$\overline{RD}$	
		$\overline{BUSRQ}$	$\overline{WR}$	
		$\overline{RESET}$	$\overline{BUSAK}$	
			$\overline{MI}$	
			$\overline{RFSH}$	

. B-8. Summary of Z80 pinout

The internal architecture of the Z80 is very similar to that of the 8080 with the most striking difference being that there are over twice as many internal registers, as shown in Fig. B-9. The instruction set of the Z80 consists of 158 instructions, including the 78 instructions of the 8080. Operating with a 4-Mhz clock, the Z80 has a minimum instruction execution time of 1 μS.

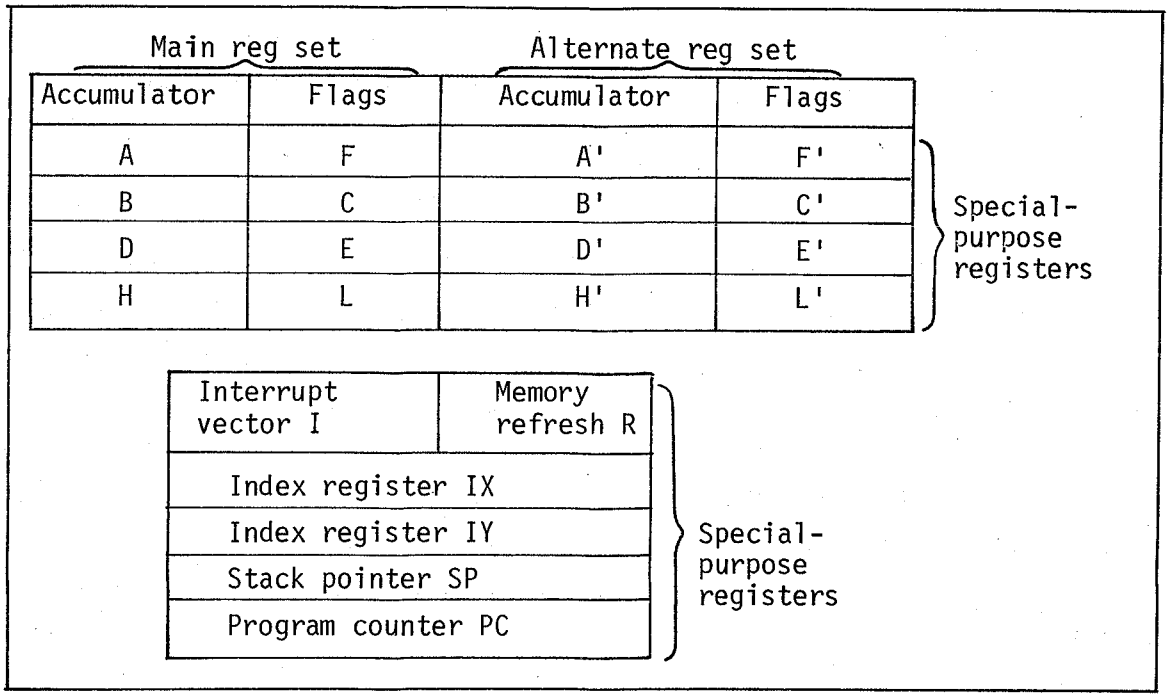


Fig. B-9. Z80 register configuration

THE 8748

A dramatic step in the evolution of microprocessors occurred with the introduction of the 8748 in February 1977. The remarkable feature of this microprocessor is that it contains 1024 bytes of programmable memory on the same chip as the microprocessor itself. The 8748 is packaged in a conventional 40-pin DIP, but is covered with a transparent quartz lid. A user can shine intense ultraviolet (UV) light through this lid to erase the stored program, and subsequently reprogram the memory of the microprocessor

Figure B-10 shows the 8784 units 40-pin package. Pins 12 to 19 form an 8-bit bidirectional data bus. There are two 8-bit bidirectional I/O ports (P10 through P17, and P20 through P27). Only a single 5-V supply is

required for operation. The chip has its own internal clock circuit requiring just a crystal connected from pin 2 to pin 3.

There is no separate address bus for the 8748. Should you wish to expand the system beyond the memory internal to the 8748, however, address information is multiplexed over the data bus at the beginning of each machine cycle. An additional 4 bits of address information are available on the four low-order bits of port 2. Thus, there is a total of 12 bits of address information allowing the direct addressing of 4K of memory.

There are six control inputs to the 8748. T0 and T1 (pins 1 and 39) are software-testable, single-bit input ports. There is an interrupt line (pin 6), a reset line (pin 4), and a ready line (pin 5). The sixth control input, external access (EA), forces the 8748 to access external, rather than internal, program memory. This is useful primarily in system debugging.

There are four control outputs for the 8748. $\overline{RD}$ indicates a read from the data bus while $\overline{WR}$ indicates a write (or output) operation on the data bus. The ALE (address latch enable) signal is used to indicate that address information is on the data bus so that it can be saved in an external latch. Finally the program store enable signal indicates that the current read operation (indicated by $\overline{RD}$ being logic 0) is fetching the next byte of the microprocessor program.

The 8748 microprocessor is built using N-channel MOS circuitry and is one of a family of processors having similar capability. A summary of the microprocessors in this family is given in Table B-1. The 8048, for example is a mask-programmed version of the 8748 that is programmed at the time of manufacturing and is not user programmable. A CMOS version of the 8048 is also available primarily for battery-powered applications. The 8748 with its on-chip memory and I/O capacity, begins to approach the ideal of a single-chip computer. A summary of the 8748 pinout is given in Fig. B-11.

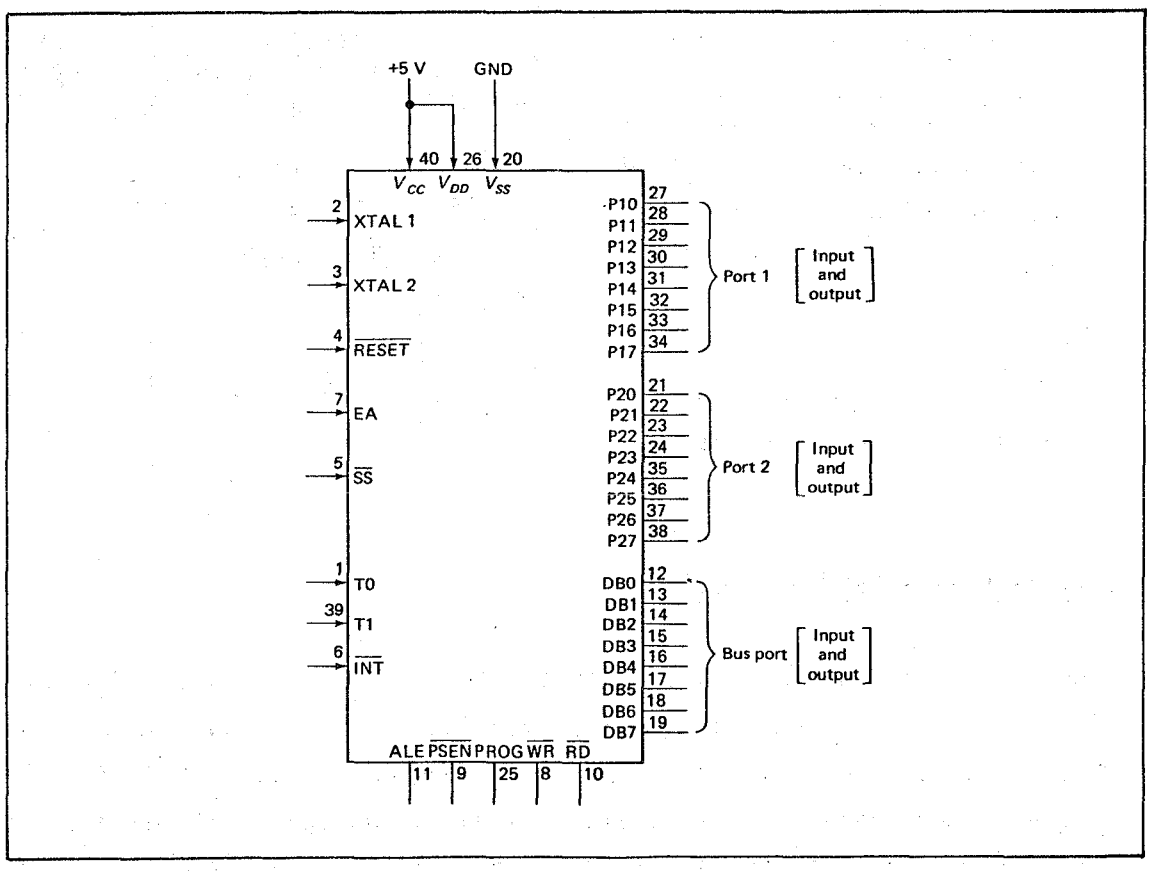


Fig. B-10. 8748 pin configuration

	8021	8035	8039	8048	8049	8748
Resident program memory (bytes)	1K ROM	None	None	1K ROM	2K ROM	1K EPROM
Resident RAM memory (bytes)	64	64	128	64	128	64
Number of I/O lines	21	27	27	27	27	27
Number of IC pins	28	40	40	40	40	40
	Lowest cost					Highest cost

Table B-1. Members of the 8748 Family of Microprocessors

Address	Data	Control bus		Power supply, V
		Inputs	Outputs	
12 Bits multiplexed on data bus and output port	Three 8-bit bidirectional ports	T0 T1 $\overline{\text{INTERRUPT}}$ $\overline{\text{RESET}}$ $\overline{\text{SS}}$ EA	$\overline{\text{RD}}$ $\overline{\text{WR}}$ ALE $\overline{\text{PSEN}}$	

Fig. B-11. Summary of 8748 pinout

MINIMAL MICROPROCESSOR SYSTEMS

Now, the various elements of microprocessor hardware discussed above can be combined to produce a complete, working microprocessor system. A very minimal system with one input port, one output port, and 1K of PROM will be considered. This minimal system is configured for each of three different microprocessors: the 8080, the Z80, and the 8748.

A diagram of a minimal 8080 system is shown in Fig. B-12. Since there is only one memory chip, one input port, and one output port, address decoding is not included in this circuit. There can be no ambiguity as to which memory chip or which input or output port is being accessed in this system. Notice that the 8080 does require a status latch, three power-supply voltages, and two externally-generated clock signals.

A minimal Z80 system is shown in Fig. B-13. The system requires one power supply voltage and one externally-generated clock signal. All required control signals are available on the Z80 control bus, and so no status latch is required in Z80 system designs.

The 8748 microprocessor has 1-K byte of PROM on the microprocessor chip itself. It also incorporates two bidirectional I/O ports. The minimal con-

figuration shown in Fig. B-14 requires very little external circuitry. The 8748, then, clearly shines in small-system design.

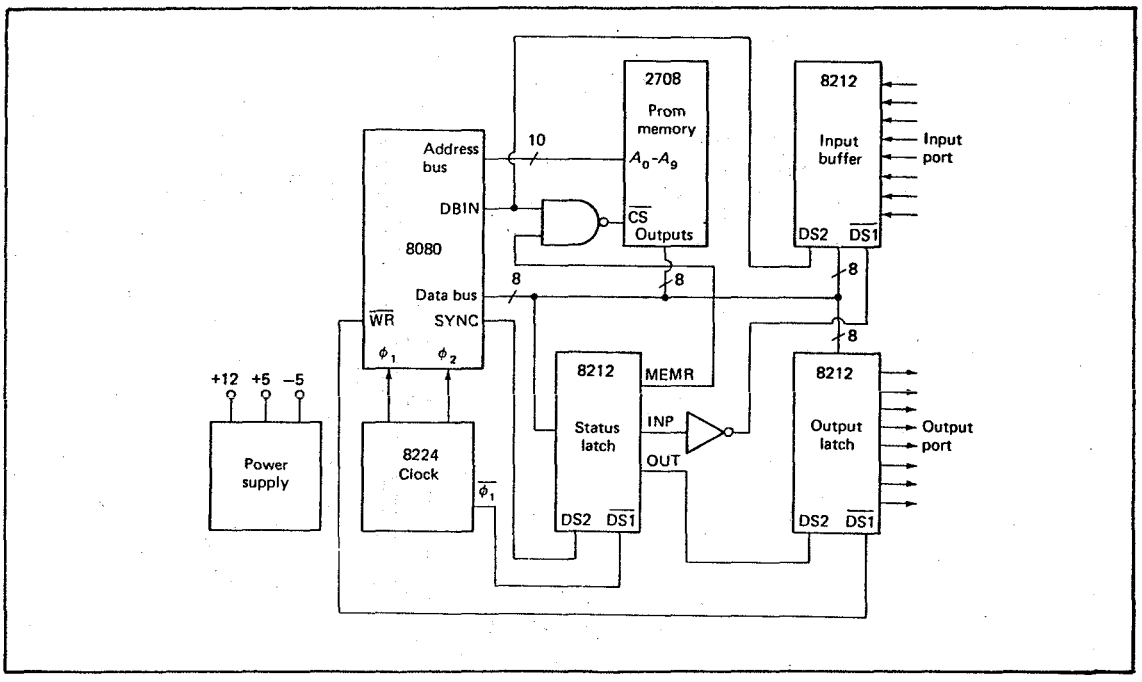


Fig. B-12. A complete microprocessor system using the 8080. Note: Since only one input port, one output port, and one memory IC are used in this system, no address decoding is required for port selection or memory chip selection.

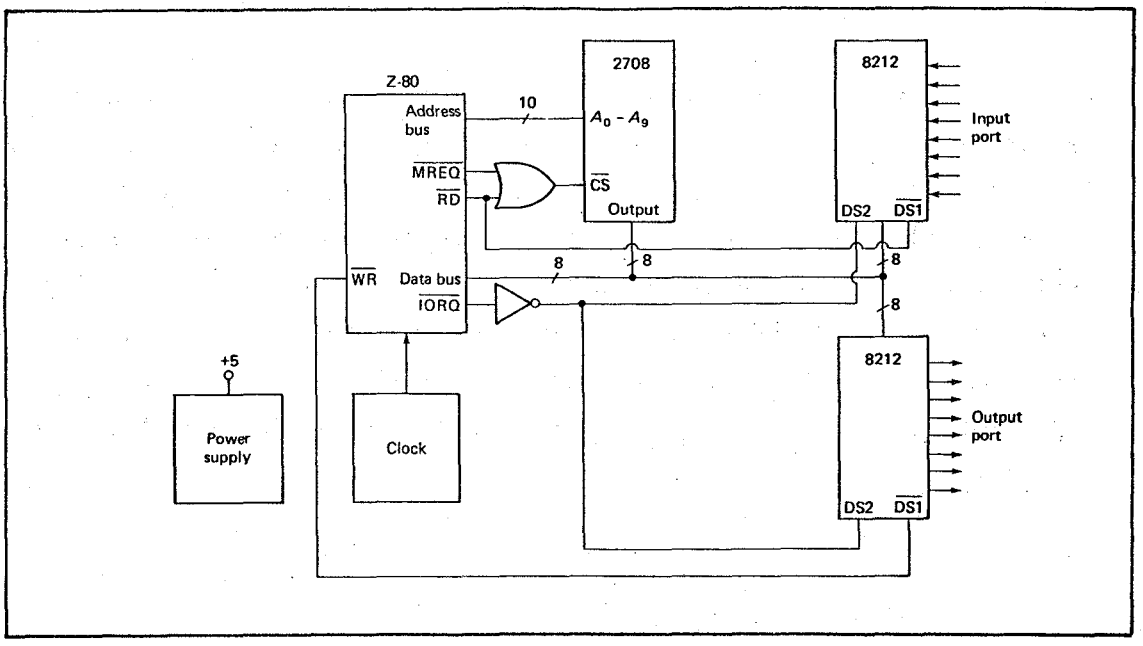


Fig. B-13. A complete microprocessor system using the Z80 microprocessor No status latch is required. The system requires a single +5-V supply and a single clock line.

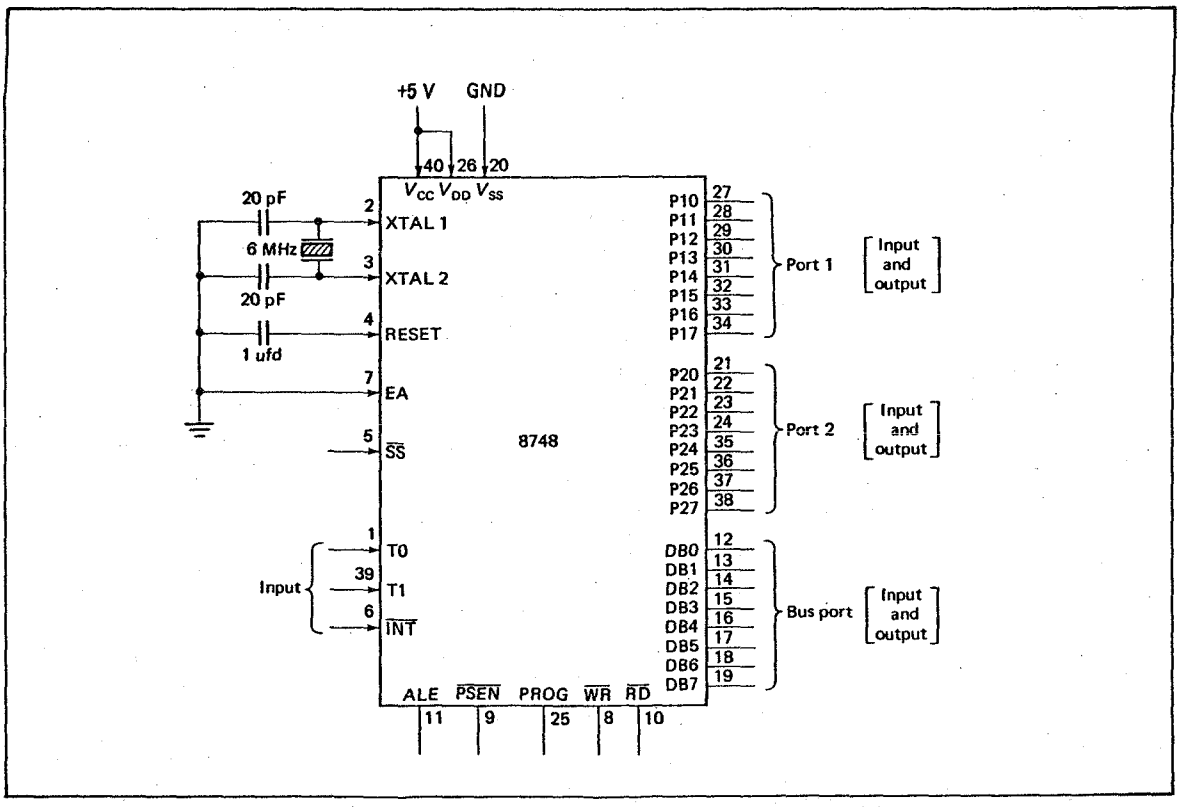


Fig. B-14. A complete microprocessor system using the 8748 microprocessor. Note: All inputs and outputs are standard TTL compatible. P1 and P2 outputs drive 5-V CMOS directly. Other require 10 to 50kΩ pull-up. XTAL: series resonant; AT cut; 1 to 6MHz.

At this stage, microprocessor evolution has branched. At the high end we find fast, high power, 16 bit microprocessor systems such as the 8086, Z8000 and recently the H16800. At the low end the all-in-one-chip microprocessor (like the 8748) has become widespread for use in consumer equipment like video-tape-recorders but also washing machines and sewing-machines. This is the kind of microprocessor that interests us now. A great many 4-bit microprocessors are now available: Very low cost types using N-MOS, and very low-power types fabricated with C-MOS technology.

C. SEMICONDUCTOR SPECIFICATIONS

In the next pages you will find some useful data of the following semiconductors :

LM311
MA311 (NSC)
HIGH SPEED COMPARATOR

Power max 30V, 187mW
Input V_{OS} 10mV
I_{OS} 70nA
I_B 300nA
V_{CM} 28V

Transfer A 106dB
response time 200nsec.

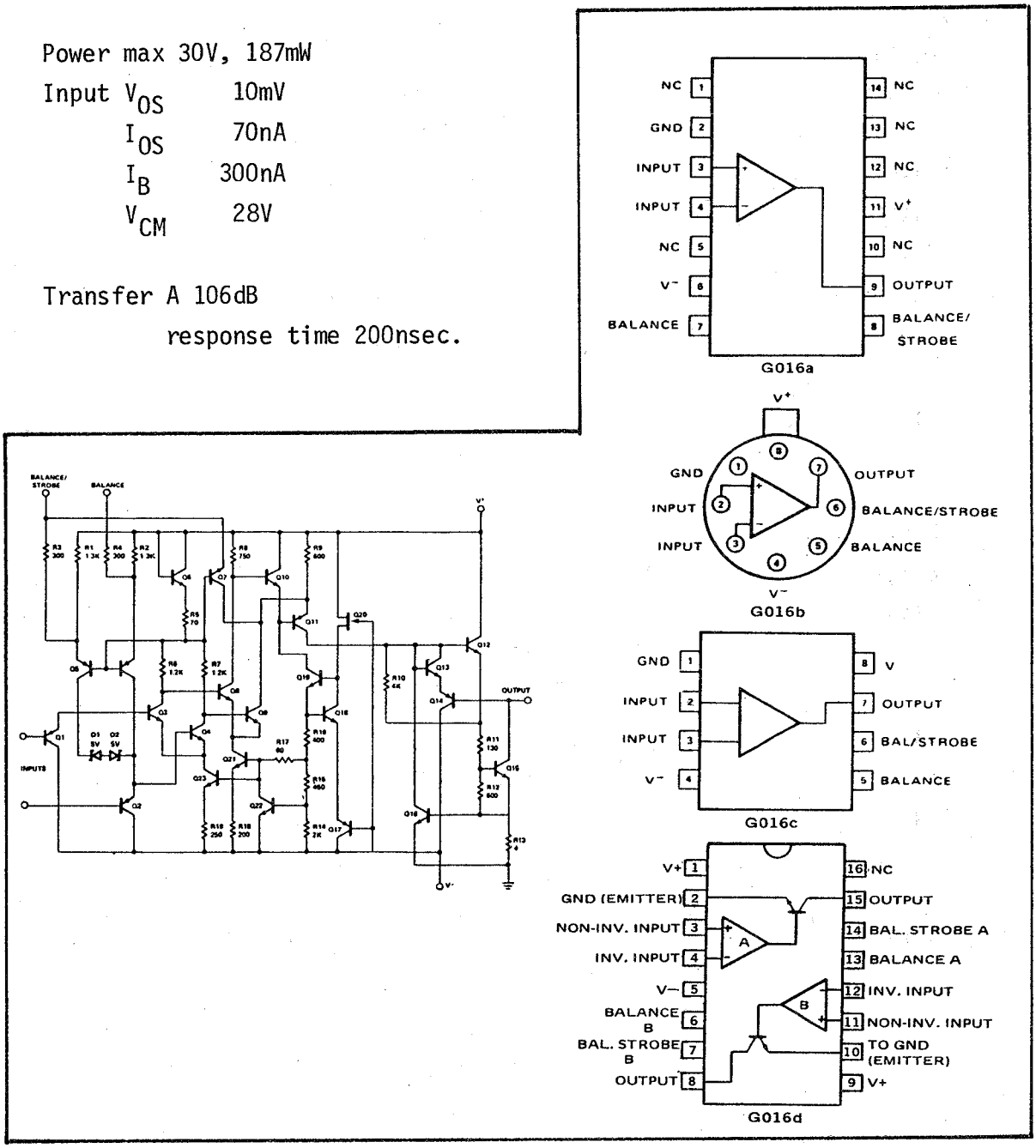


Fig. C-1

μPC4558C (NEC)	8-759-145-58	(D)
equivalents :		
NJM4558DFA	8-759-700-58	(D)
HA17458GS(HITACHI)	8-759-374-58	(E)
μPC1458C (NEC)	8-759-114-58	(D)

HIGH-PERFORMANCE DUAL OP-AMP

Power	max.	30V	
	max.	170mW	
	ICC	5mA	(open output current consumption)
Input	V_{OS}	6mV	
	I_{OS}	200nA	
	I_{BIAS}	500nA	
	VCM	24V	(common mode range)
Transfer	A_{OL}	86dB	(open loop gain)
slew rate		1V/μs	
	CMRR	70dB	

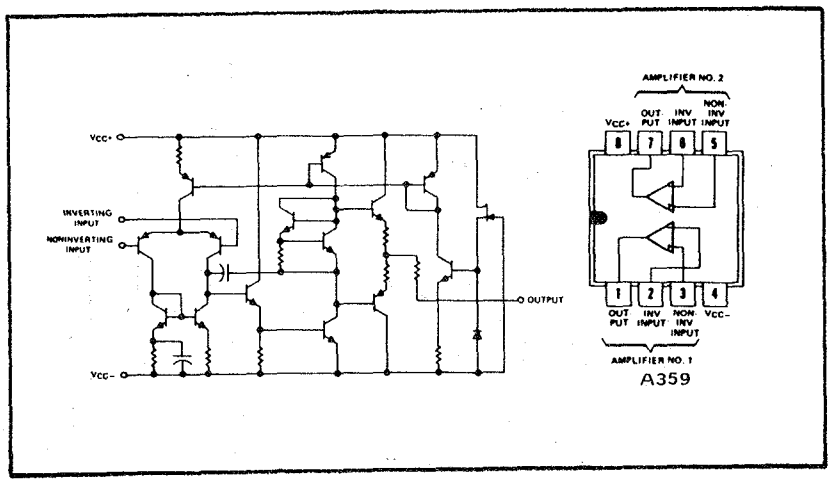


Fig. C-2.

QUAD COMPARATOR OPEN-COLL. OUTPUT

Power	max.	36V
	max.	570mW
	ICC	2mA
Input	V_{OS}	5mV
	I_{OS}	50nA
	I_B	250nA
	V_{CM}	-0.3 ∼ V_{CC}
Output	Isink	16mA
Transfer	A	100dB @ 15kΩ

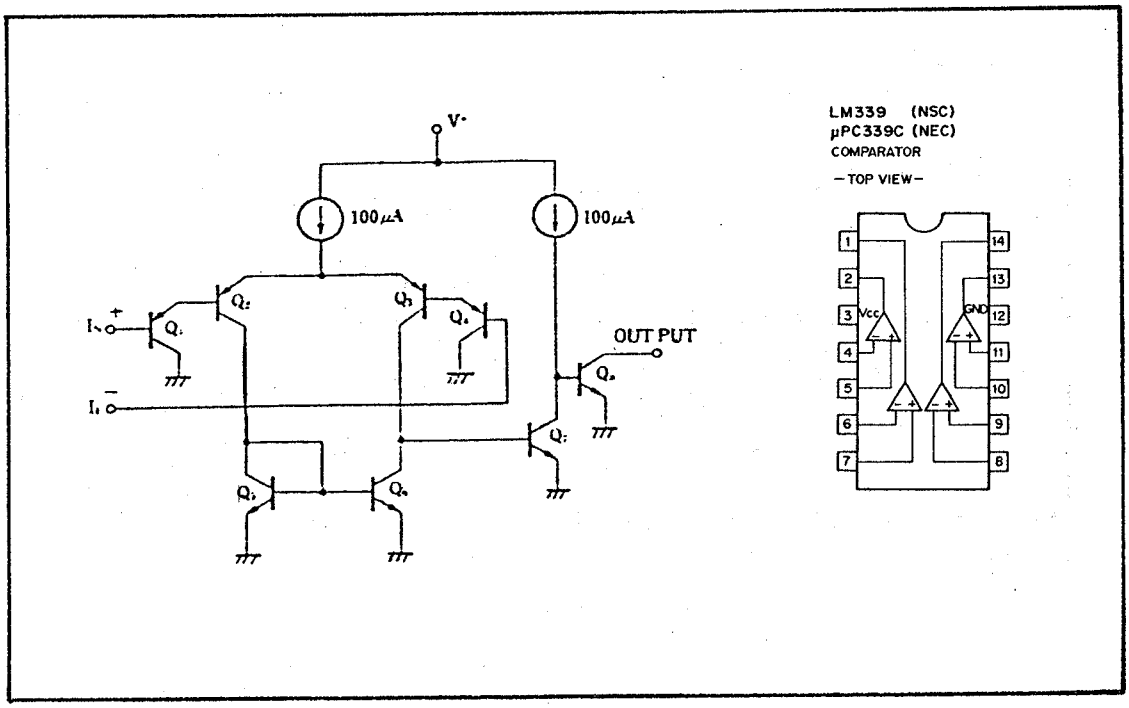


Fig. C-3.

TL064C (TI) 8-759-900-64

QUAD OP-AMP (J FET INPUT)

Power	max. 30V, 15mW	
Input	V_{OS}	7.5mV
	V_{drift}	10nV/°C
	I_B	7nA
	I_{OS}	3nA
	V_{CM}	24V
	Z in diff	1TΩ
Transfer	BW3dB	1MHz
	A_{OL}	72dB
	slew rate	3.5V/µs
	CMRR	80dB

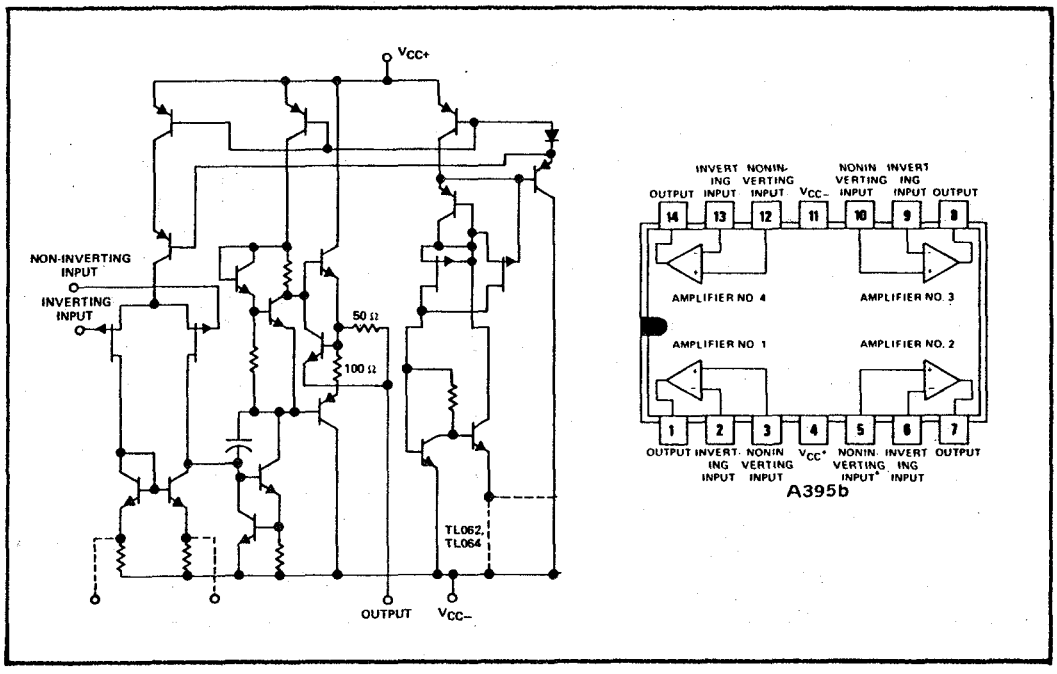


Fig. C-4.

TL072CP (TI) 8-759-990-72

OP AMP, LOW NOISE, JFET INPUT

Power	30V,	150mW
Input	Vdrift	10μV/°C
	OS	13mV
	I_{OS}	2nA
	BIAS	7nA
	VCM	20V
	Zdiff	$10^{12}\Omega$
Output	24V	a 10k
Transfer	f3dB	3MHz
	A_{OL}	88dB
	slew	13V/μs
	CMRR	70dB

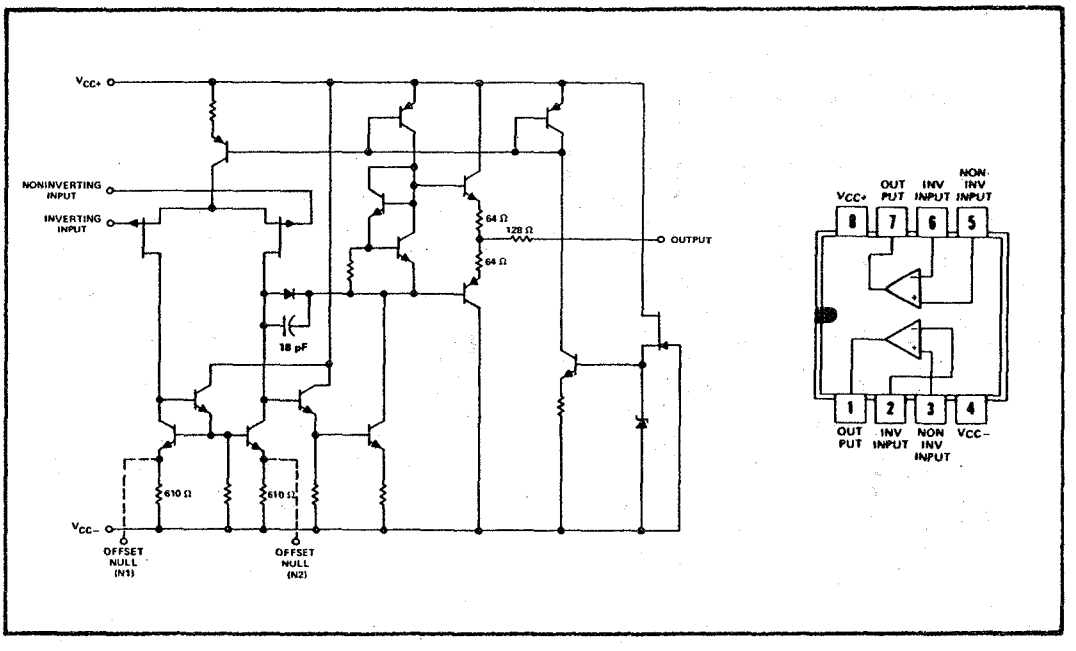


Fig. C-5.

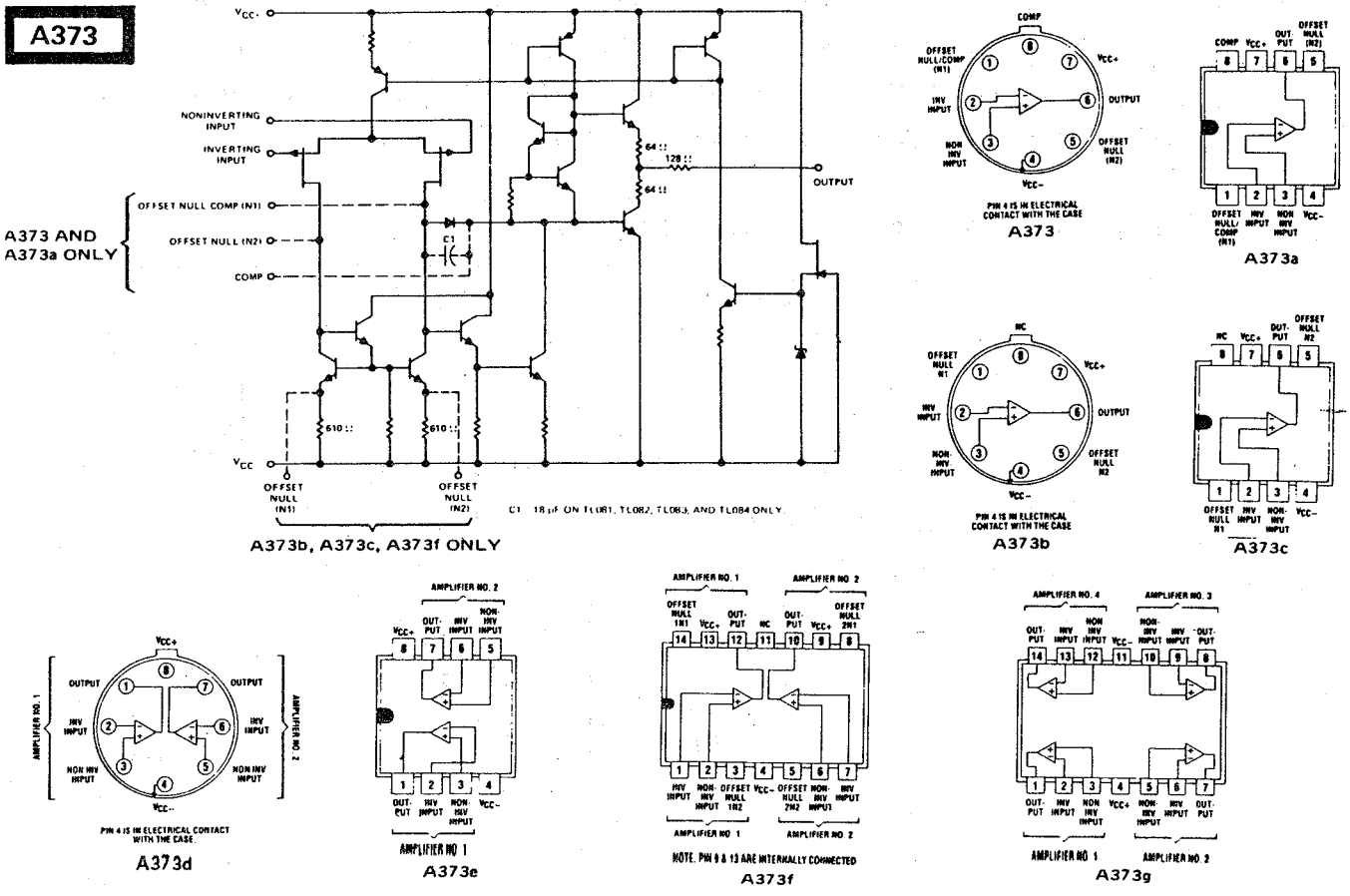
TL081CP

082CP(TI)	8-759-990-82
083CN	
084CN(TI)	8-759-990-84

DUAL
QUAD OP-AMP, JFET INPUT

Power	30V, 0.17W
Input	drift 10μV/°C, V_{OS} 20mV
	I_{OS} 5nA, I_{BIAS} 10nA
	CMrange 20V
	Z in diff 1.0 TΩ
Output	$24V_{pp}$ @ 10k
	BW 3dB 3MHz
	A_{OL} 80dB
	slew 12V/μs
	CMRR 70dB

Fig. C-6



4051B - 8-Channel Analog Multiplexer/Demultiplexer

Description

The 4051B is an 8-channel Analog Multiplexer/Demultiplexer with three Address inputs (A_0 - A_2), an active LOW Enable input ($\overline{E}$), eight independent inputs/outputs (Y_0 - Y_7) and a common input/output (Z).

The 4051B contains eight bidirectional analog switches, each with one side connected to an independent input/output (Y_0 - Y_7) and the other side connected to a common input/output (Z). With the Enable input ($\overline{E}$) LOW, one of the eight switches is selected (low impedance ON state) by the three Address inputs (A_0 - A_2). With the Enable input ($\overline{E}$) HIGH, all switches are in the high impedance OFF state, independent of the Address inputs.

V_{DD} and V_{SS} are the two supply voltage connections for the digital control inputs (A_0 - A_2, $\overline{E}$). Their voltage limits are the same as for all other digital CMOS. The analog inputs/outputs (Y_0 - Y_7, Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. V_{DD} - V_{EE} may not exceed 15V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

. ANALOG OR DIGITAL MULTIPLEXER/DEMULTIPLEXER
. COMMON ENABLE INPUT (ACTIVE LOW)

PIN NAMES

Y_0 - Y_7	Independent inputs/outputs
A_0 - A_2	Address inputs
$\overline{E}$	Enable input (active LOW)
Z	Common input/output

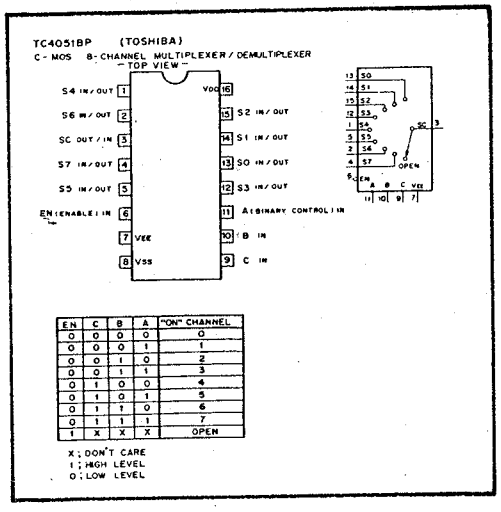


Fig. C-7.

4053B - Triple 2-Channel Analog Multiplexer/Demultiplexer

Description

The 4053B is a Triple 2-Channel Analog Multiplexer/Demultiplexer with a common Enable input ($\overline{E}$). Each Multiplexer/Demultiplexer has two independent inputs/outputs (Y_0, Y_1), a Common input/output (Z), and a Select input (S). Each Multiplexer/Demultiplexer contains two bidirectional analog switches, each with one side connected to an Independent input/output (Y_0, Y_1)and the other side connected to a Common input/output (Z). With the Enable input ($\overline{E}$) LOW, one of the two switches is selected (low impedance, ON state) by the Select input (S). With the Enable input ($\overline{E}$) HIGH, all switches are in the high impedance OFF state, independent of the Select inputs (S_a - S_c).

V_{DD} and V_{SS} are the two supply voltage connections for the Digital Control inputs (S_a - S_c, $\overline{E}$). Their voltage limits are the same as for all other digital CMOS. The analog inputs/outputs Y_0, Y_1, Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. V_{DD} - V_{EE} may not exceed 15V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

. ANALOG OR DIGITAL MULTIPLEXER/DEMULTIPLEXER
. COMMON ENABLE INPUT (ACTIVE LOW)

PIN NAMES

Y_{0a} - Y_{0c}, Y_{1a} - Y_{1c}	Independent input/outputs
S_a - S_c	Select inputs
$\overline{E}$	Enable input (Active LOW)
Z_a - Z_c	Common input/outputs

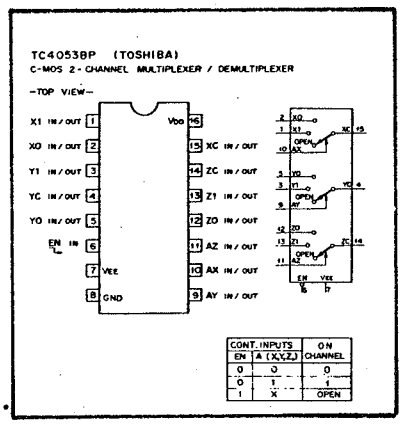


Fig. C-8.

ANALOG SWITCH CHARACTERISTICS

DC CHARACTERISTICS: V_{DD} as shown, V_{EE} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
R_{ON}	ON Resistance	XC		95	900		55	380		35	210	Ω	MIN	V_{is} = V_{DD} to V_{EE} Note 2
				100	1000		65	500		40	280		25°C	
				125	1100		100	600		65	340		MAX	
		XM		90	850		50	340		30	190	Ω	MIN	
				100	1000		65	500		40	280		25°C	
				150	1150		110	660		70	370		MAX	
ΔR_{ON}	"Δ" ON Resistance Between Any Two Channels			25			10			5		Ω	25°C	Note 2
I_Z	OFF State Leakage Current, All Channels OFF	XC						800				nA	25°C	$\overline{E}$ = V_{DD}, V_{SS} = $V_{DD}/2$, V_{is} = V_{DD} or V_{EE}, V_{os} = V_{EE} or V_{DD}
		XM						80						
	Any Channel OFF	XC						100						$\overline{E}$ = V_{SS} = $V_{DD}/2$, V_{is} = V_{DD} or V_{EE}, V_{os} = V_{EE} or V_{DD}
		XM						10						
I_{DD}	Quiescent Power Supply Dissipation	XC			20			40			80	μA	MIN, 25°C	V_{SS} = V_{EE}, All inputs at V_{DD} or V_{EE}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{EE} = 0 V, T_A = 25 C (See Note 3)

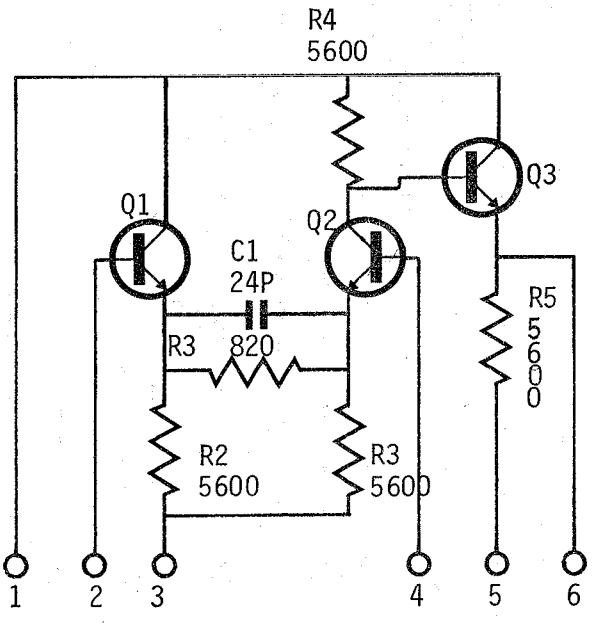
SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay,		25			10			6		ns	C_L = 50 pF, R_L = 200 kΩ, $\overline{E}$ = V_{SS} = V_{EE}, A_n or V_{is} = V_{DD} or V_{EE} Note 5
t_{PHL}	Input to Output		10			6			4			
t_{PLH}	Propagation Delay,		170			95			80		ns	
t_{PHL}	Address to Output		210			125			95			
t_{PZL}	Output Enable Time		185			95			75		ns	C_L = 50 pF, R_L = 1 kΩ, E or A_n = V_{SS} = V_{EE}, V_{is} = V_{DD} or V_{EE} Note 5
t_{PZH}			205			105			85			
t_{PLZ}	Output Disable Time		1250			1130			1080		ns	
t_{PHZ}			1240			1120			1070			
	Distortion, Sine Wave Response		0.2			0.2			0.2		%	R_L = 10 kΩ, V_{SS} = $V_{DD}/2$, $\overline{E}$ = V_{EE}, V_{is} = $V_{DD}/2$ (sine wave) p-p, f_{is} = 1 kHz
	Crosstalk Between Any Two Channels					1					MHz	R_L = 1 kΩ, $\overline{E}$ = V_{EE}, V_{is} = $V_{DD}/2$ (sine wave) p-p at -40 dB, V_{SS} = $V_{DD}/2$, 20 Log_{10} (V_{os}/V_{is}) = -40 dB
	OFF State Feedthrough					1					MHz	R_L = 1 kΩ, V_{SS} = $V_{DD}/2$, $\overline{E}$ = V_{DD}, V_{is} = $V_{DD}/2$ (sine wave) p-p, 20 Log_{10} (V_{os}/V_{is}) = -40 dB
f_{MAX}	ON State Frequency Response		13			40			70		MHz	R_L = 1 kΩ, $\overline{E}$ = V_{SS}, V_{is} = $V_{DD}/2$ (sine wave) p-p, V_{SS} = $V_{DD}/2$, 20 Log_{10} (V_{os}/V_{os} @ 1 kHz) = -3 dB

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. E V_{SS} R_L 10 kΩ, any channel selected and V_{SS} V_{EE} or $V_{DD}/2$.
3. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
4. V_{is}/V_{os} is the voltage signal at an Input/Output terminal (Y_n/Z_n).
5. V_{IN} V_{DD} (Square Wave), Input transition times 20 ns, R_L 10 kΩ.
6. In certain applications, the current through the external load resistor (R_L) may include both V_{DD} and signal line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 2, 4, 5, 12, 13, 14, or 15 the voltage drop across the bidirectional switch must not exceed 0.5 V at T_A 25 C, or 0.3 V at T_A 25 C. No V_{DD} current will flow through R_L if the switch current flows into terminal 3.

BX305A

VIDEO AMPLIFIER

Power from +9V, -6V
ICC 3.5mA
IEE 3.5mA



R1	5600 Ω	± 10%
R2	5600 Ω	± 10%
R3	820 Ω	± 5%
R4	5600 Ω	± 5%
R5	5600 Ω	± 10%
C1	24P	± 10%
Q1	F	3,4
Q2	F	3,4
Q3	F	3,4
R3, R4		± 5%

Fig. C-9.

DUAL SAWTOOTH VOLTAGE GENERATOR
(FOR STATIC DEFLECTION)

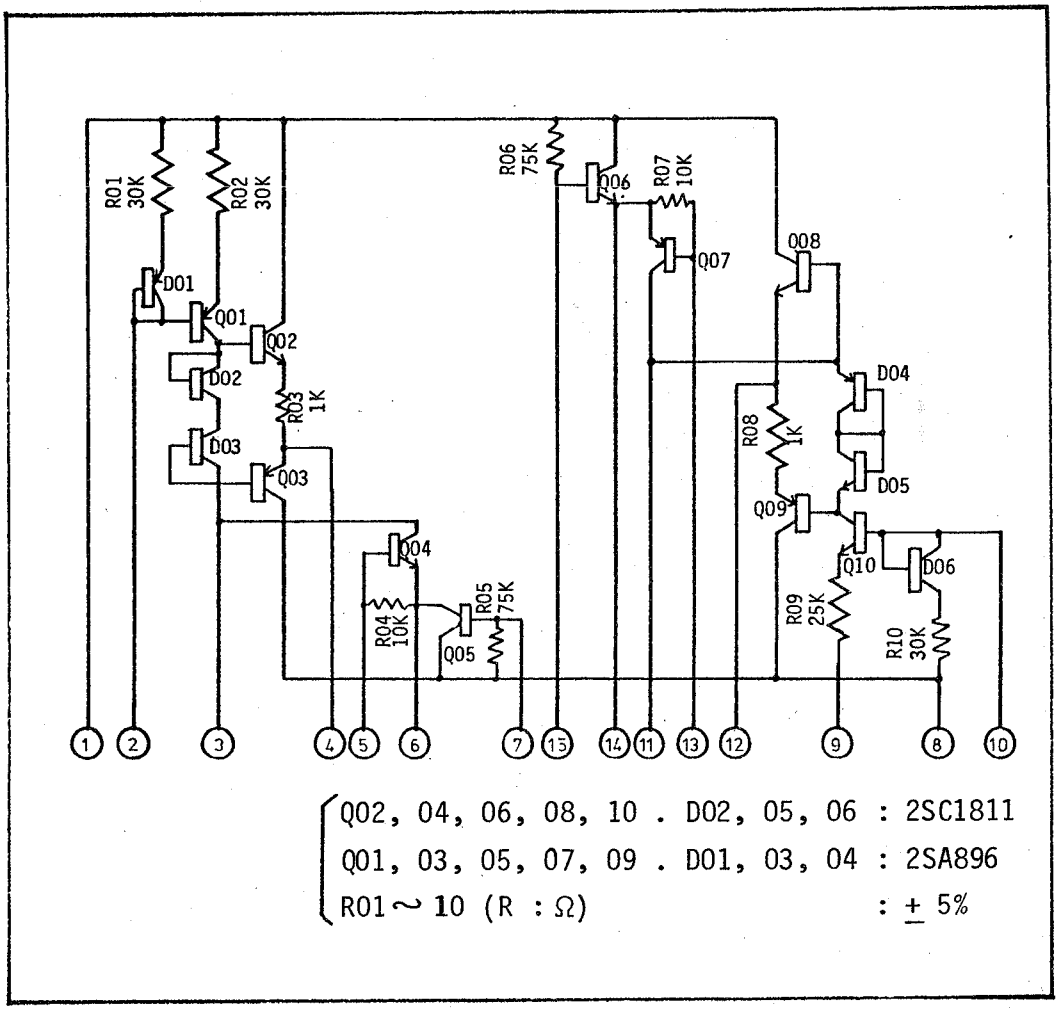


Fig. C-10.

SAWTOOTH FORMER FOR INDEX CORRECTION

Power V_{CC} +9V (8.5mA)
V_{EE} -7V(-8.0mA)

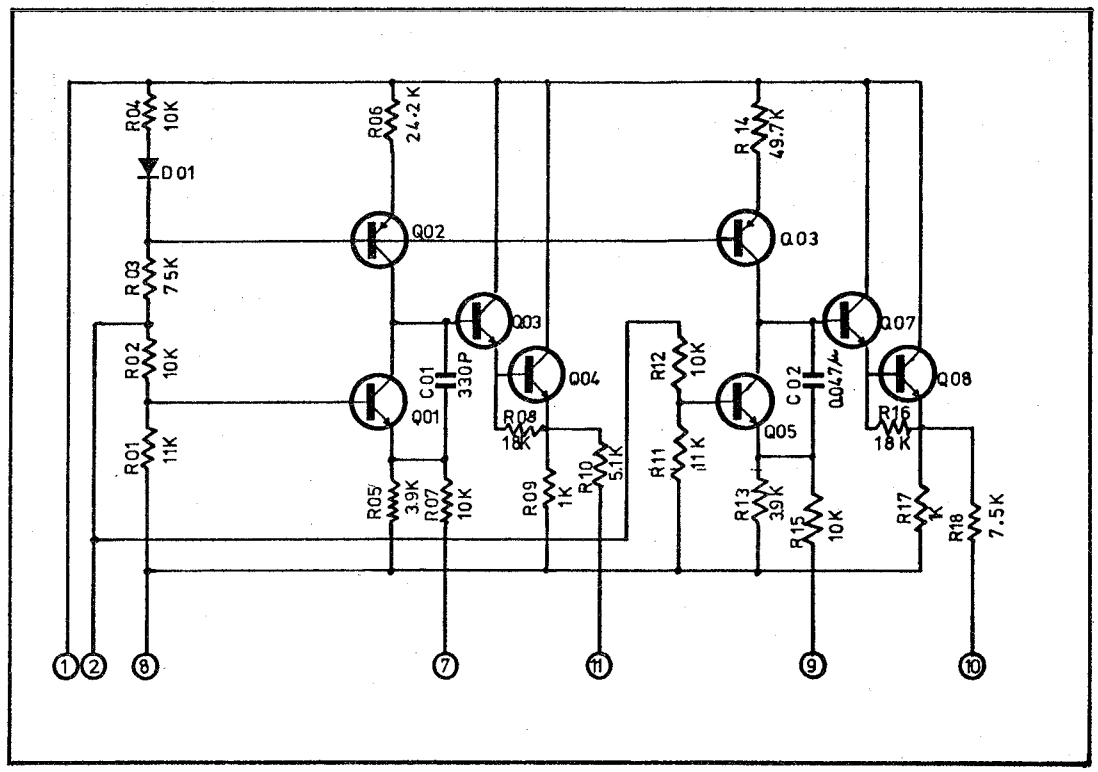


Fig. C-11.

CX518 (SONY)

M54890L (MITSUBISHI)

INTERFACE CIRCUIT BETWEEN VTR & CAMERA

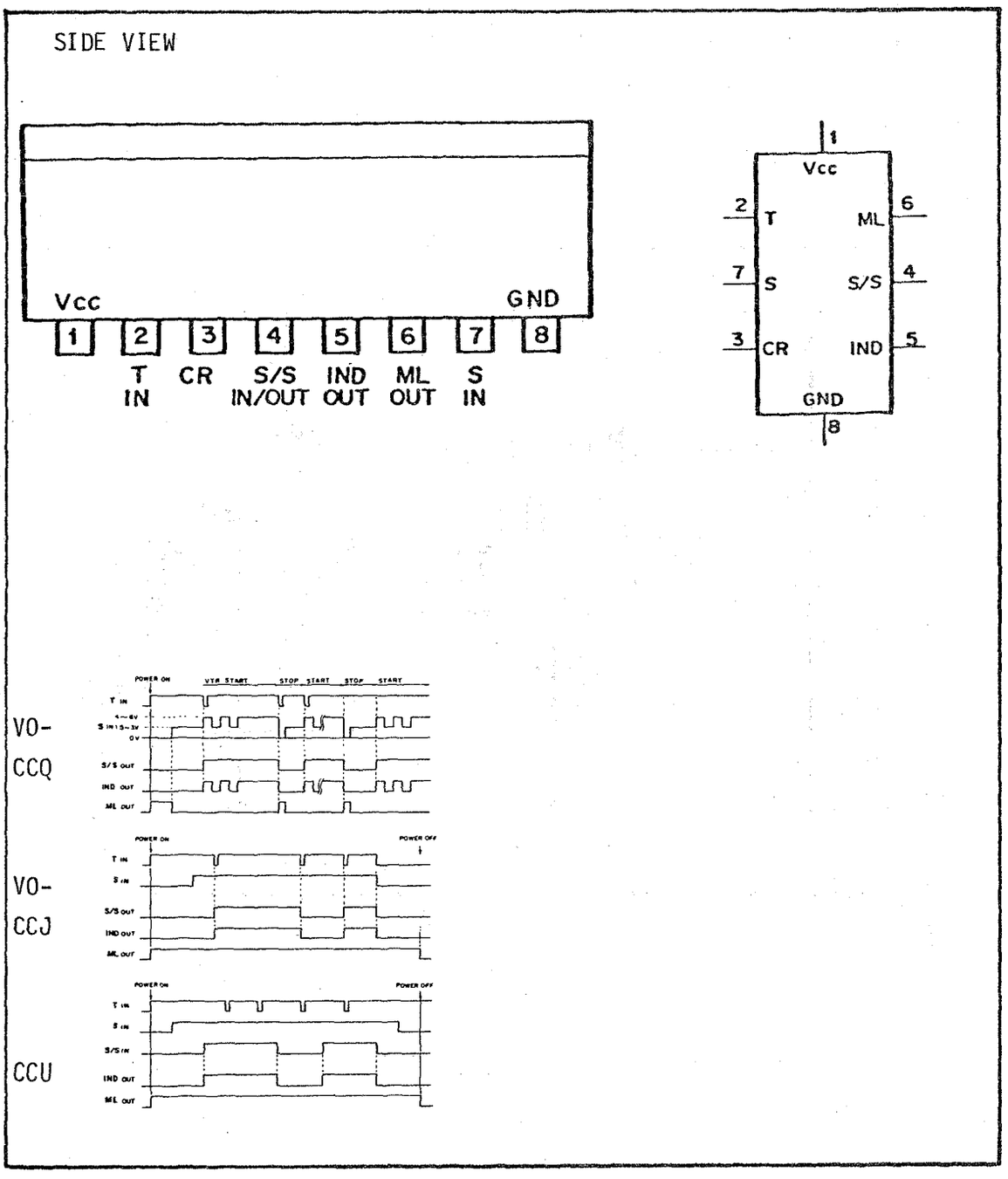


Fig. C-12. Block Diagram

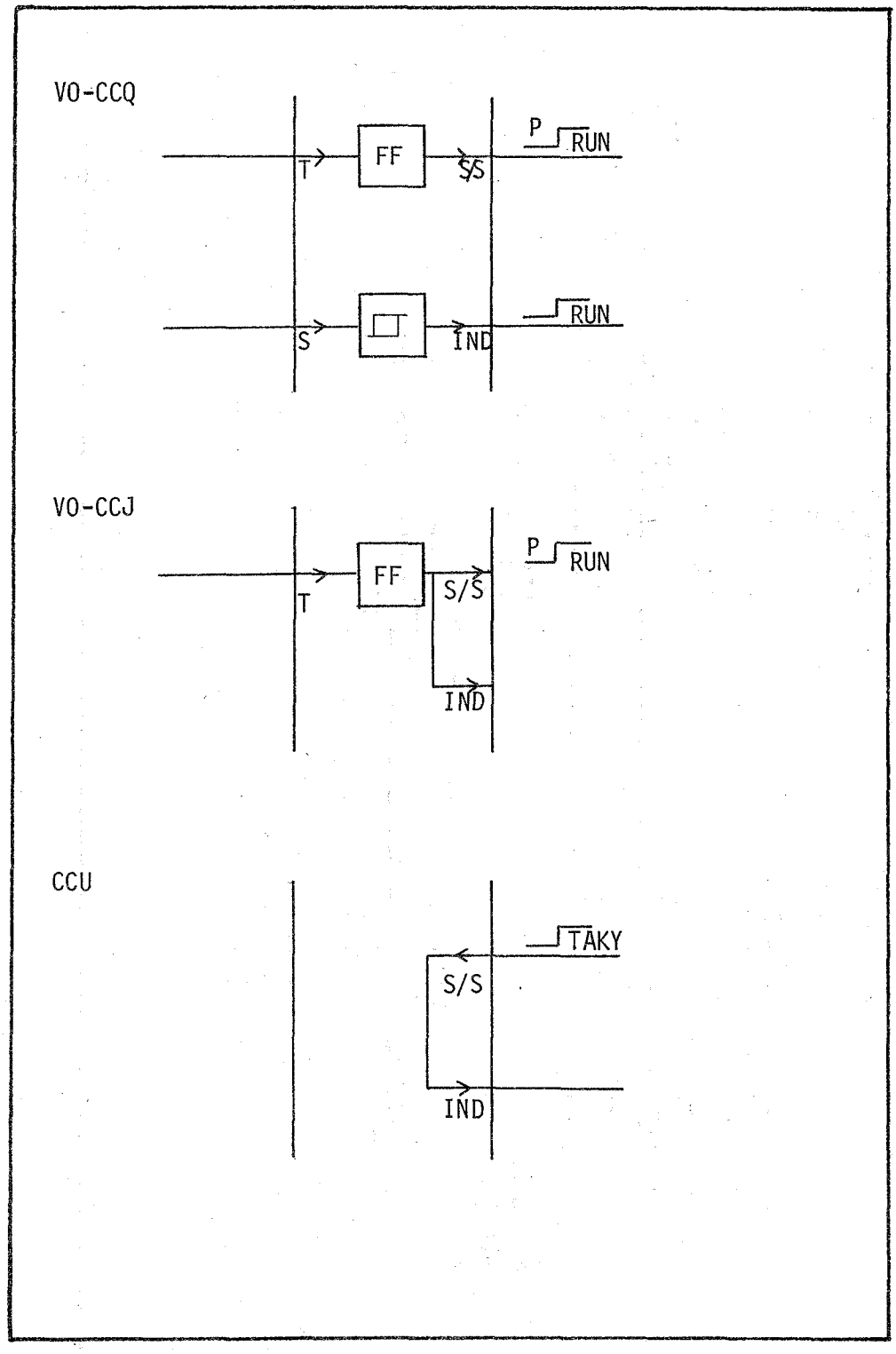

VO-CCQ
T
FF
S/S
P
RUN
S
IND
RUN
VO-CCJ
T
FF
S/S
P
RUN
IND
CCU
TAKY
S/S
IND

Fig. C-13.

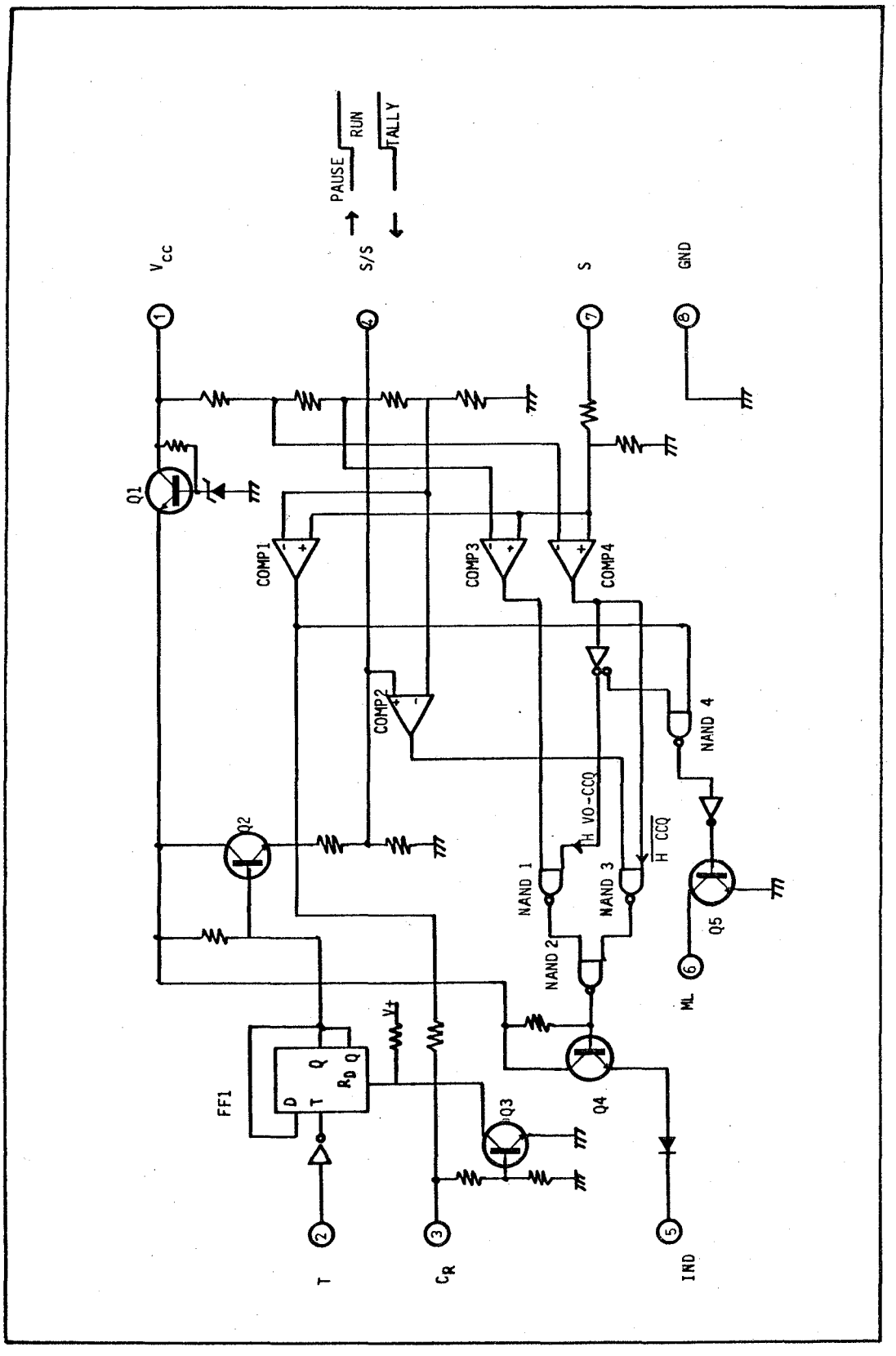
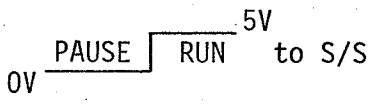


Fig. C-14. CX518 Functional Block Diagram.

Always S > 1V → COMP 1-OUT H
→ Q3 ON, FF - RESET input L
→ trigger possible



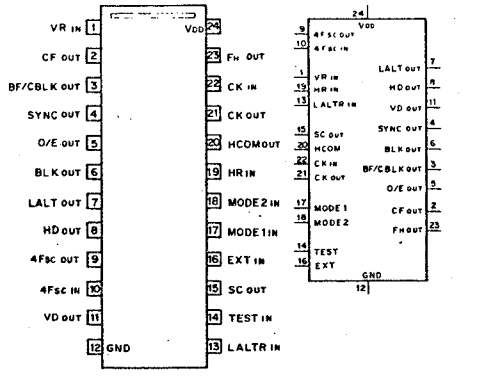
CCQ S ⩽ 5V
→ COMP 4-OUT L
S signal through COMP 3 (2.5 < ref < 5V)
and NAND 1/2, Q4 to IND pin 5.
with S > 1V : COMP1-OUT H } Q5 ON → ML L
COMP4-OUT L }

CCJ S 12V
→ COMP4-OUT H
S/S through COMP2 (ref ≅ 1V), NAND 3, Q4 to IND pin 5.
ML H

CCU same as CCJ
but now C_R input must be held low
→ FF reset.
S/S acts as input and goes to IND (Tally)
ML H

CX773A (SONY)

C-MOS SYNC GENERATOR (NTSC, PAL, PAL-M, SECAM)
DIL 24p
Power max. 7.5V
25mA at 5V



O/E : ODD/EVEN FIELD
CF : COLOUR FRAME PULSE
HCOM : H COMPARATOR

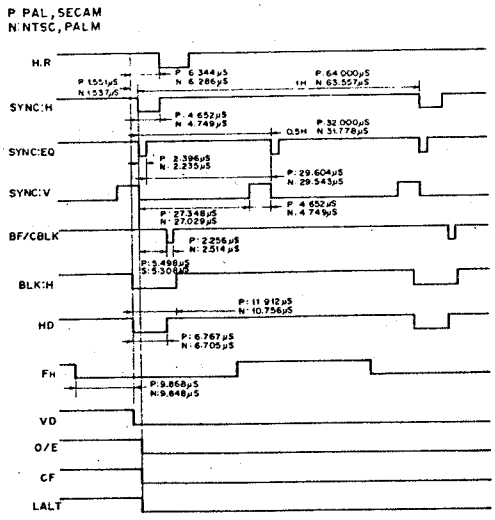
SYSTEM	4Fsc	CLOCK
NTSC	910 FH	910FH
PAL	1135FH+2Fv	908FH
PALM	909FH	910FH
SECAM	——	908FH

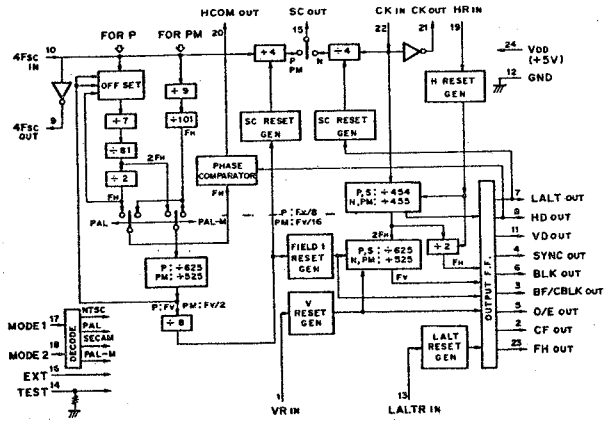
INTUPS MODE 1	INTUPS MODE 2	SYSTEM
0	0	NTSC
0	1	SECAM
1	0	PALM
1	1	PAL

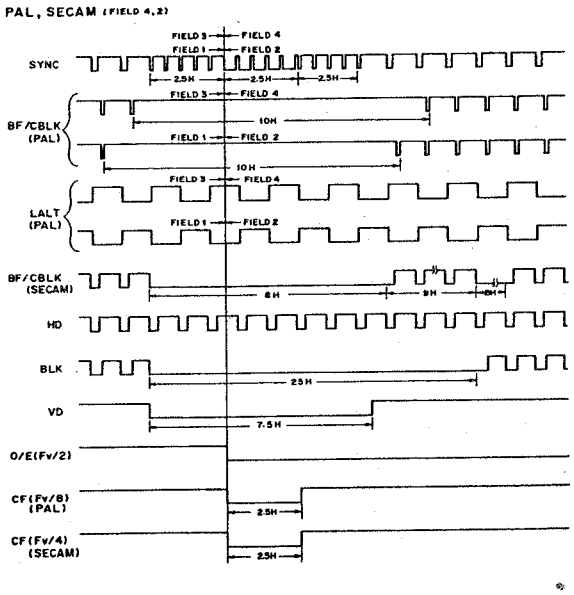
"1" : VDD
"0" : GND

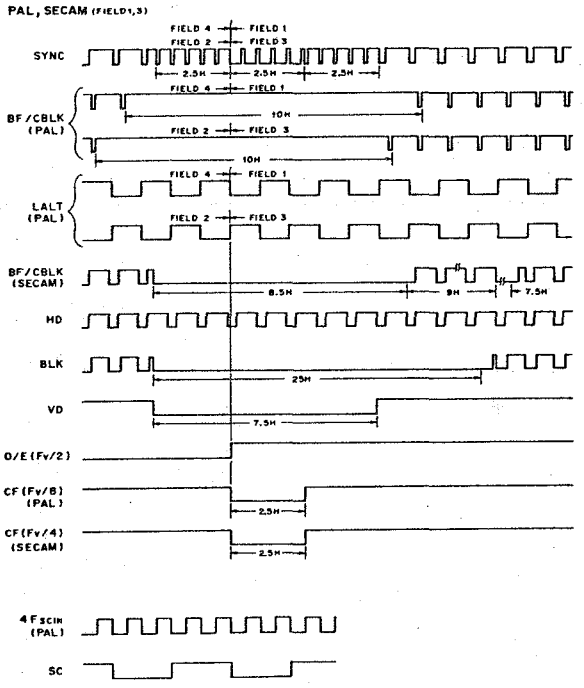
INTUPS EXT	INTUPS TEST	FUNCTION
0	0	INTERNAL
0	1	INVALID
1	0	EXT
1	1	TEST

TEST "0" : OPEN (INTERNALLY PULLED DOWN)









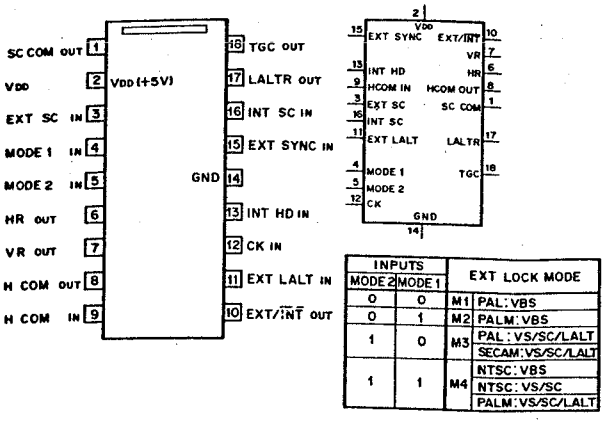
Functions :

- CDWN from clock to B/W sync
- " " 4 f_{sc} to f_{sc}
- " " 4 f_{sc} to f_H
- $f_H \varphi$ comparator

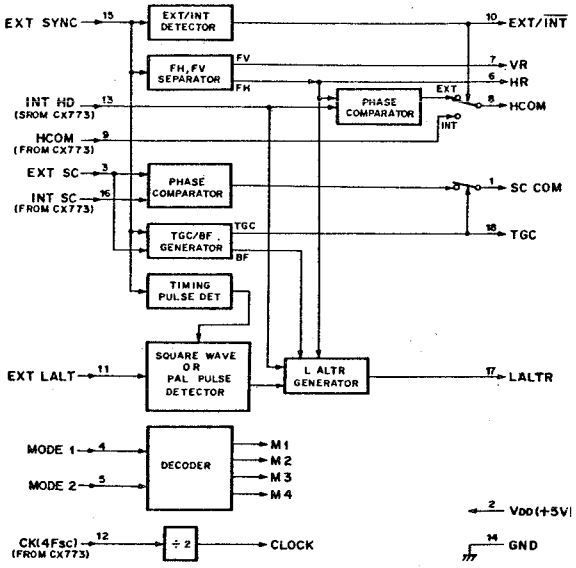
Fig. C-15.

CX7903 (SONY)

CMOS GEN-LOCK ADAPTOR FOR CX773



INPUTS		EXT LOCK MODE	
MODE 2	MODE 1		
0	0	M1	PAL:VBS
0	1	M2	PALM:VBS
1	0	M3	PAL:VS/SC/LALT
			SECAM:VS/SC/LALT
1	1	M4	NTSC:VBS
			NTSC:VS/SC
			PALM:VS/SC/LALT

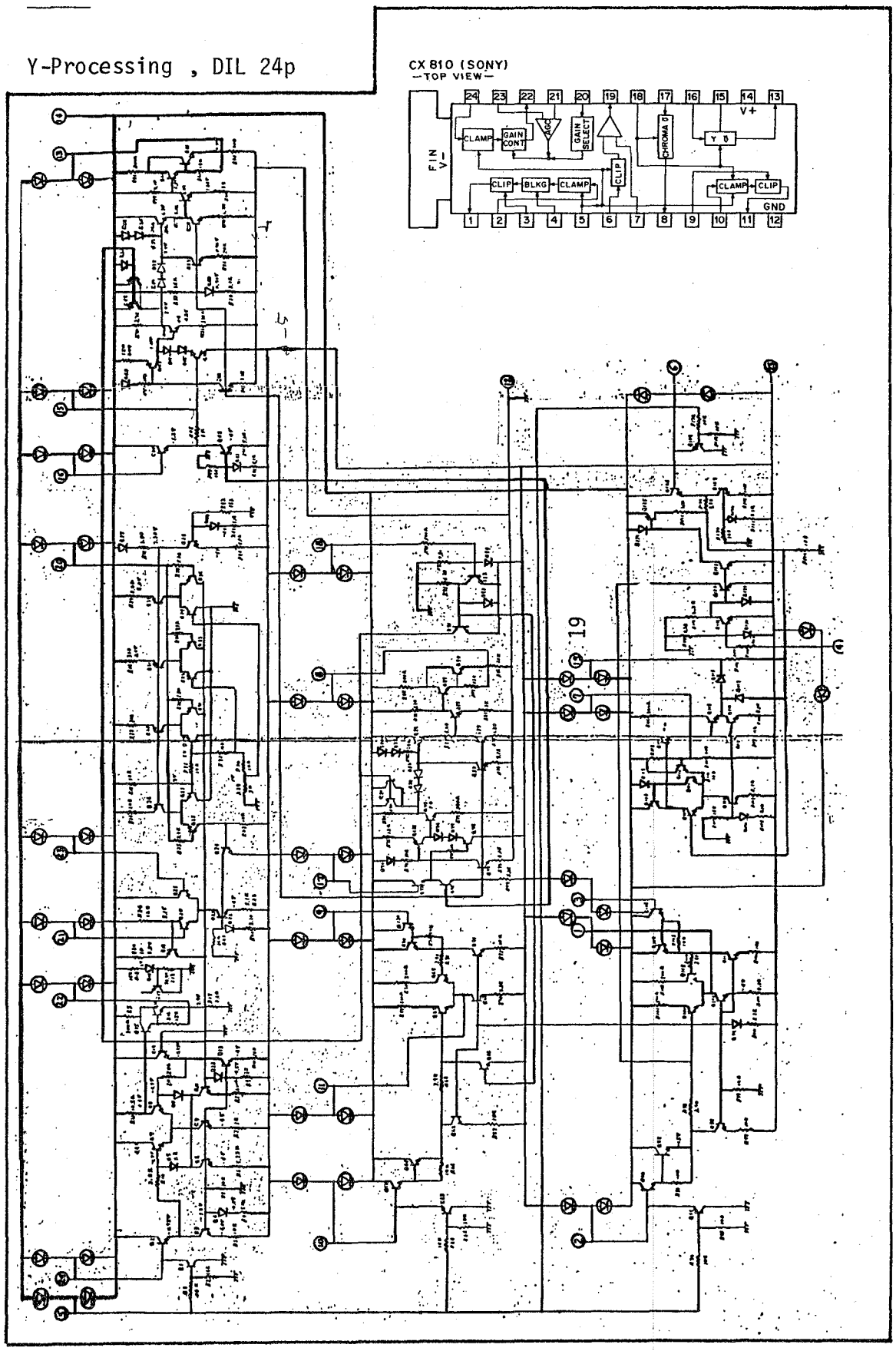


Functions : external detector
VD/HD separator
f_H φ comparator
H loop error switch
SC φ comparator
burst sampling gate
L-ALT reset generator

C-16.

CX810

Y-Processing , DIL 24p

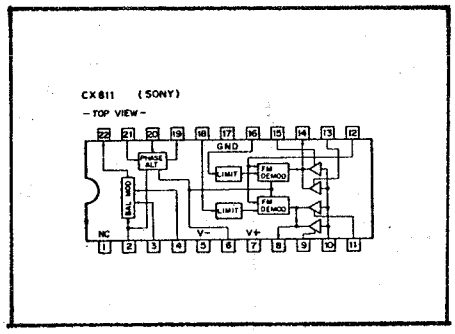


C-17.

CX811

COLOUR DEMODULATOR
INDEX CORRECTION AND ALTERNATOR

DIL 22p



C-18.

CX814

VIDEO OUTPUT, FADER

monolithic, bipolar
DIL 14p

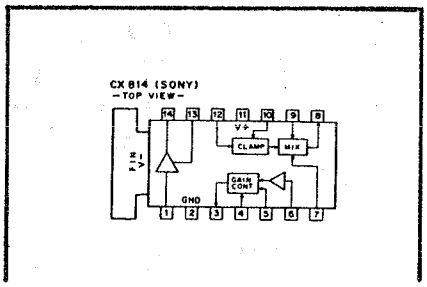
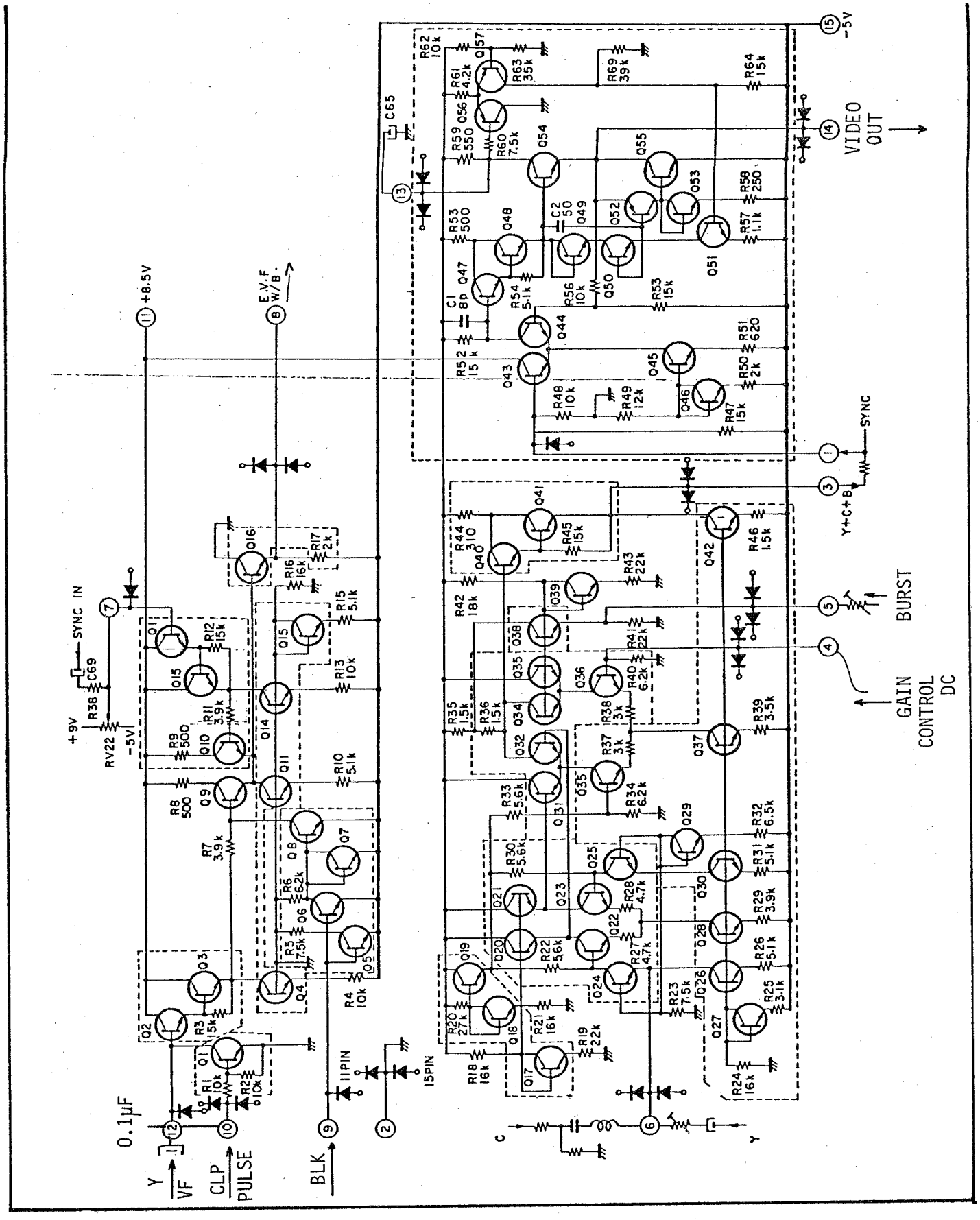


Fig. C-19.


+8.5V
E.V.F W/B.
-5V
VIDEO OUT
SYNC
Y+C+B
BURST
GAIN CONTROL DC
SYNC IN
+9V
-5V
RV22
0.1μF
Y/VF
CLP PULSE
BLK
11PIN
15PIN
C
Y

CX815

APERTURE CORRECTION AMPLIFIER

monolithic, bipolar
DIL

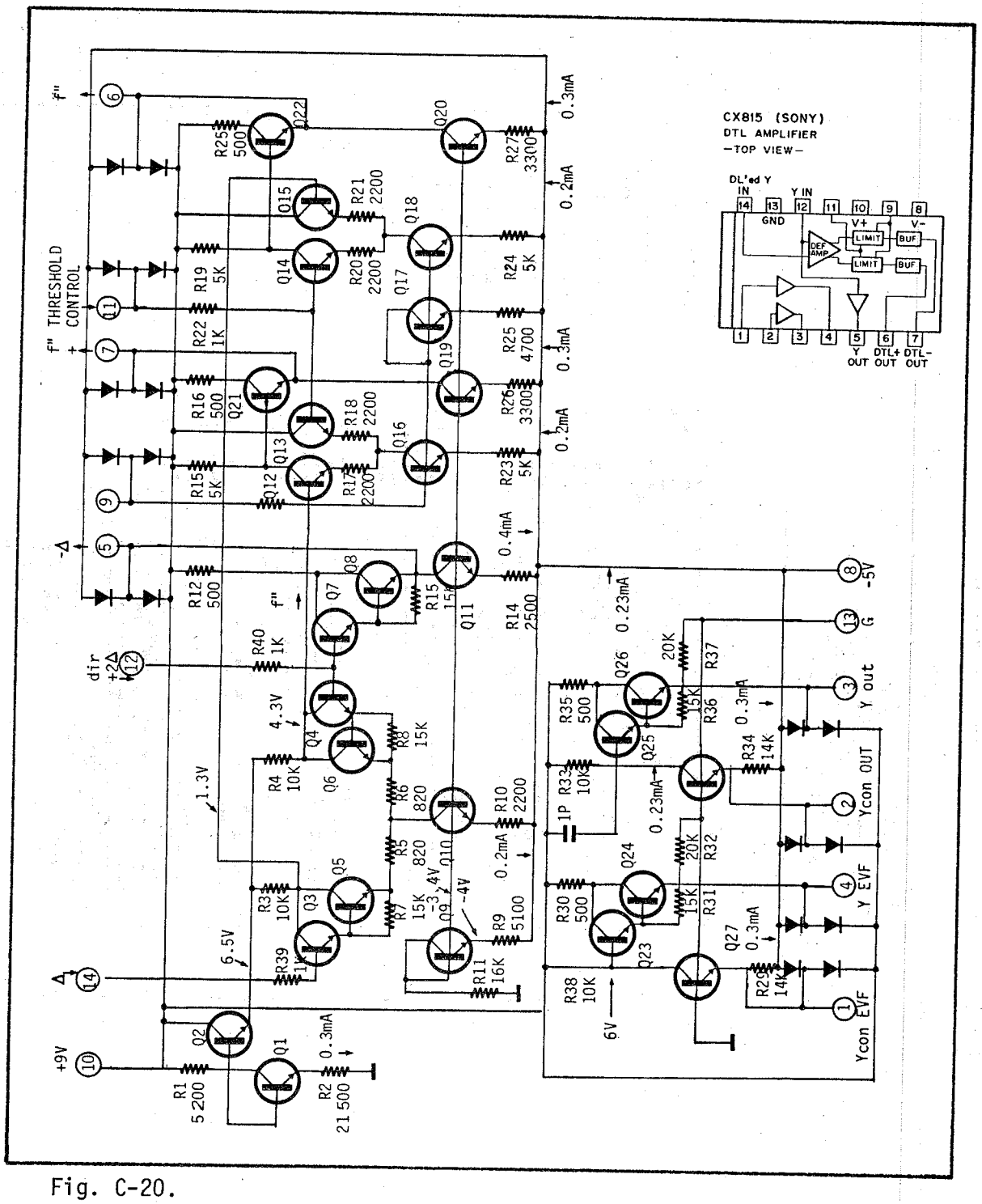


Fig. C-20.

CX816

DELAY LINE DRIVER

monolithic, bipolar

ICC 6.3mA

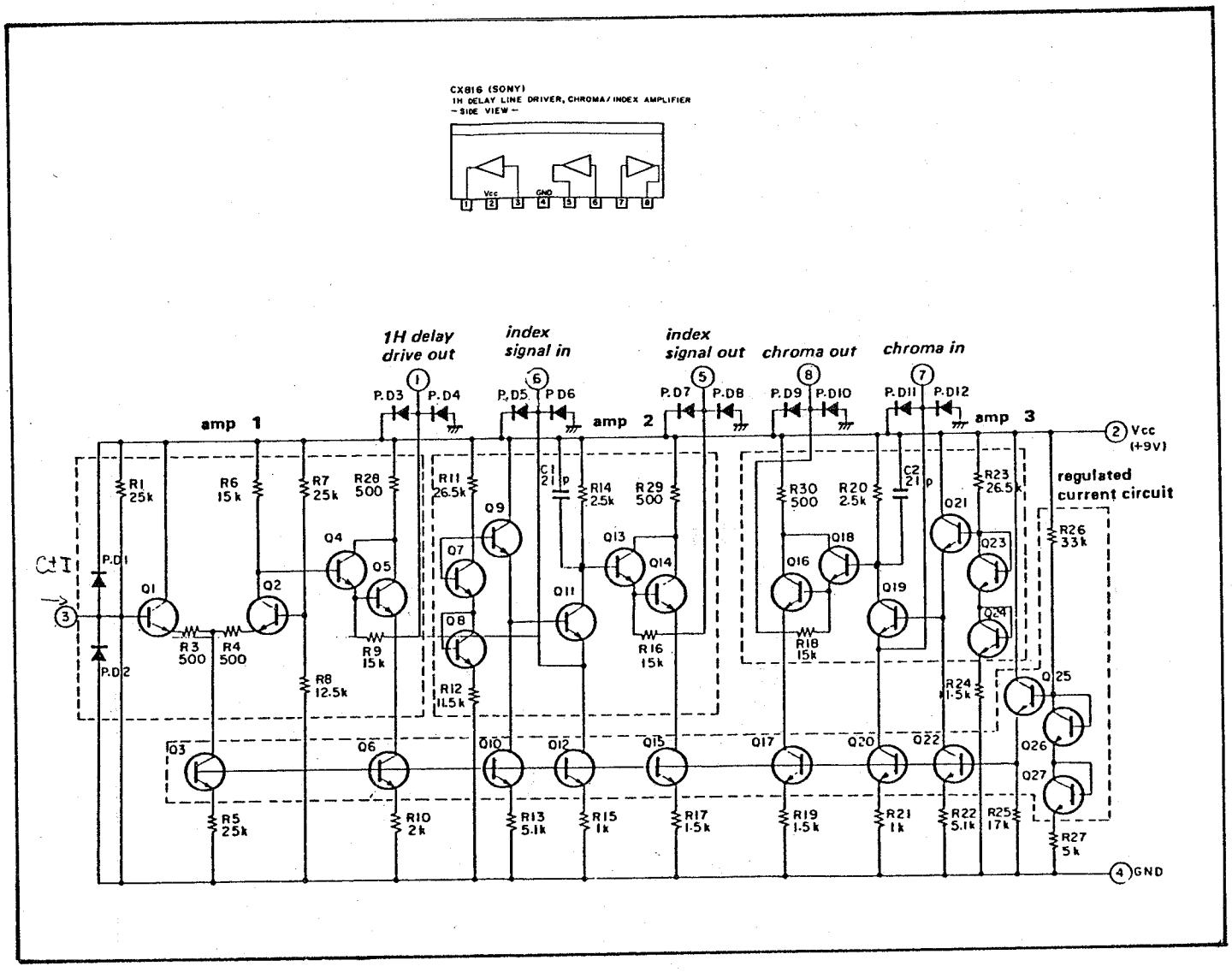


Fig. C-21.

2SK152

JFET
N-channel
Epitaxial planar

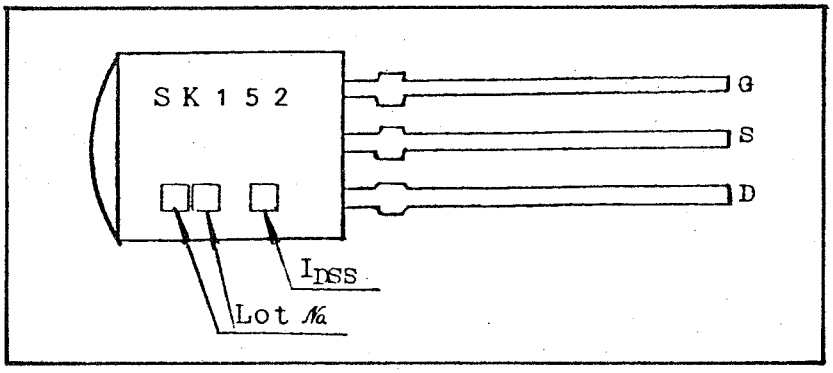


Fig. C-22.

VARIABLES	CONDITION	MIN	TYPE	MAX	UNIT
V_{DGO}	I_D = 10μA	15			V
V_{SGO}	I_D = 10μA	15			V
I_{GSS}	V_{GS} = 7V, V_{DS} = 0			2	nA
I_{DSS}	V_{DS} = 5V V_{GS} = 0	9.5		42	mA
V_P	V_{DS} = 5V I_D = 100μA	0.55		2.0	V
gmo	V_{DS} = 5V V_{GS} = 0V f=1kHz	21	30		mΩ
Ciss	V_{DS} = 5V V_{GS} = 0V f=1kHz		8	9	pF

RANK	I_{DSS} (V_{DS} = 5V, V_{GS} = 0V)	V_P (V_{DS} = 5V, I_D = 100μA)	gmo (V_{DS} = 5V f = 1kHz, V_{GS} = 0V)
1	- 9.5 ～14.8mA	0.55 ～ 1.0V	21m ～
2	13.4 ～21.0	0.65 ～1.26	23.5～
3	19.0 ～ 30.2	0.85 ～1.6	25.5～
4	27.4 ～42.0	1.05 ～ 2.0	27.5～

VARIABLES	CONDITION	TYPE	UNIT
gm	V_{DS} = 5V I_D = 10mA f=1kHz	25	mΩ
Ciss	V_{DS} = 5V I_D = 10mA f=1MHz	7.2	pF
I_G	V_{DG} = 5V I_D = 10mA	40	pA
ris	V_{DS} = 5V I_D = 10mA	3.5	kΩ
Cis	f = 100MHz	7.2	pF
ros		3	kΩ
Cos		2.5	pF
PG	V_D = 5V I_D = 10mA	15	dB
NF	f = 100MHz	1.8	dB
e_n	V_{DS} = 5V I_D = 10mA f=1kHz Rg=0Ω	1.2	$nV/\sqrt{Hz}$
Cdg	V_{DS}= 5V V_{GS} = 0V f=1MHz	2.0	pF

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